

ZZZ
PCB
Part Number = DAZ0C600200

Compal Confidential

NEW75 Schematics Document

AMD Danube

Champlain Processor with RS880M/SB820/Madison VGA

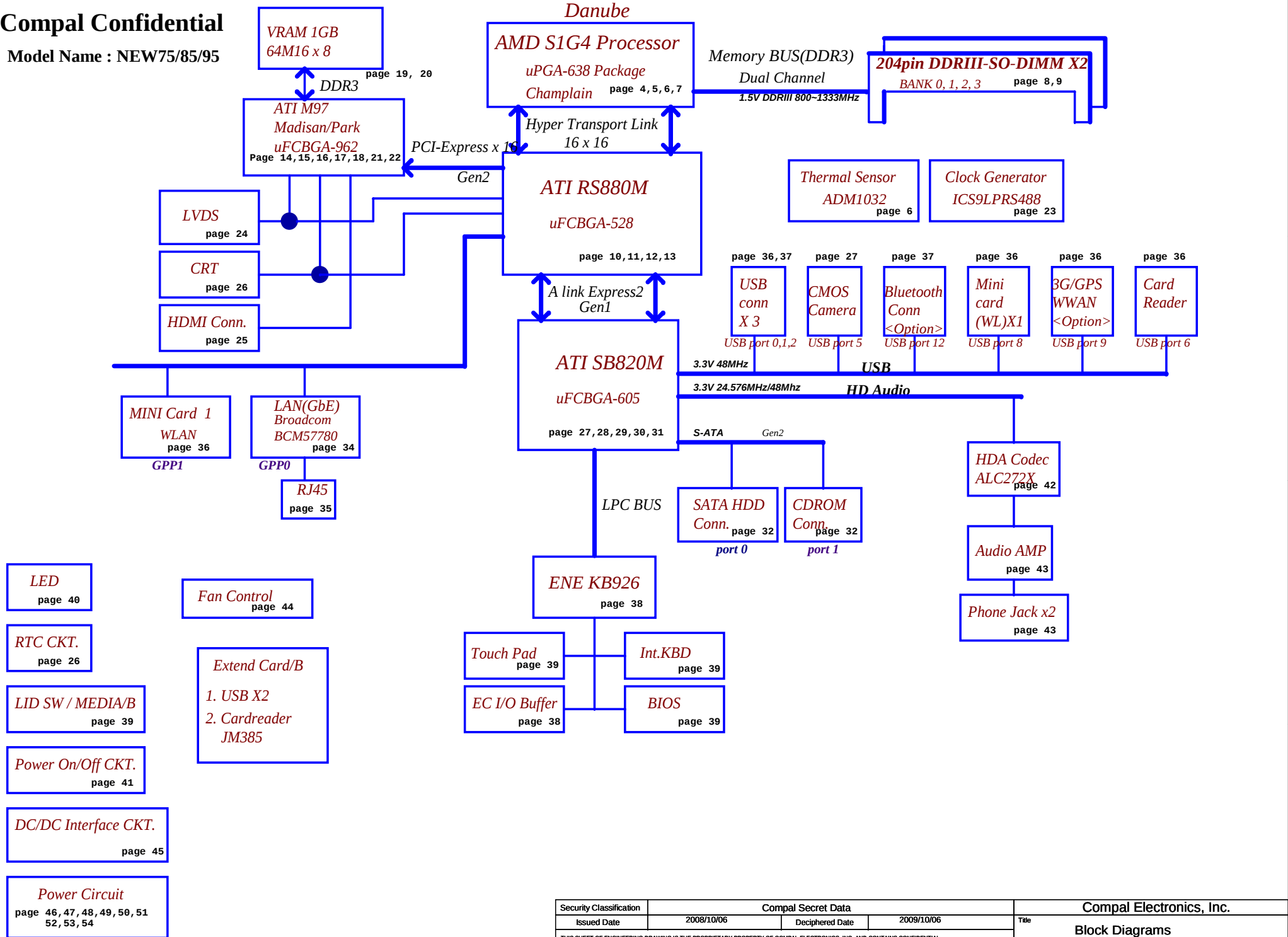
2010-03-22

LA5911P REV: 1.0

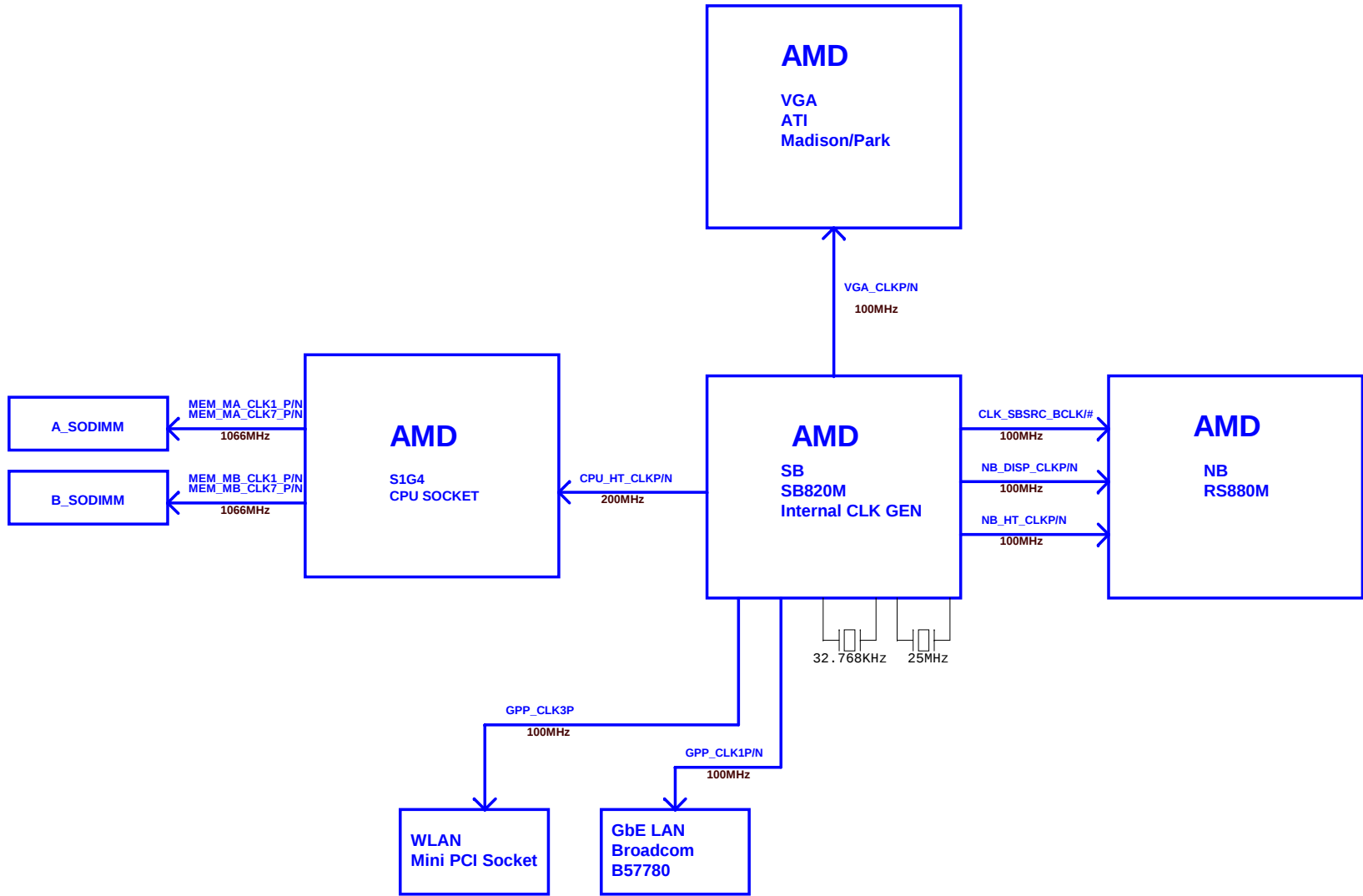
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				Date: Tuesday, March 23, 2010	Rev 0.1
				Sheet 1 of 55	

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Model Name : NEW75/85/95



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				Date: Monday, March 22, 2010	Sheet 2 of 55
				Rev 0.1	



Security Classification		Compal Secret Data		Title CLOCK DISTRIBUTION	
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				Date: Monday, March 22, 2010	Rev 0.1
				Sheet 3 of 55	

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

External PCI Devices

EC SM Bus1 address

EC SM Bus2 address

SB820
SM Bus 1 address

BOM Config

Board ID / SKU ID Table for AD channel

BOARD ID Table

BTO Option Table

Project ID Table

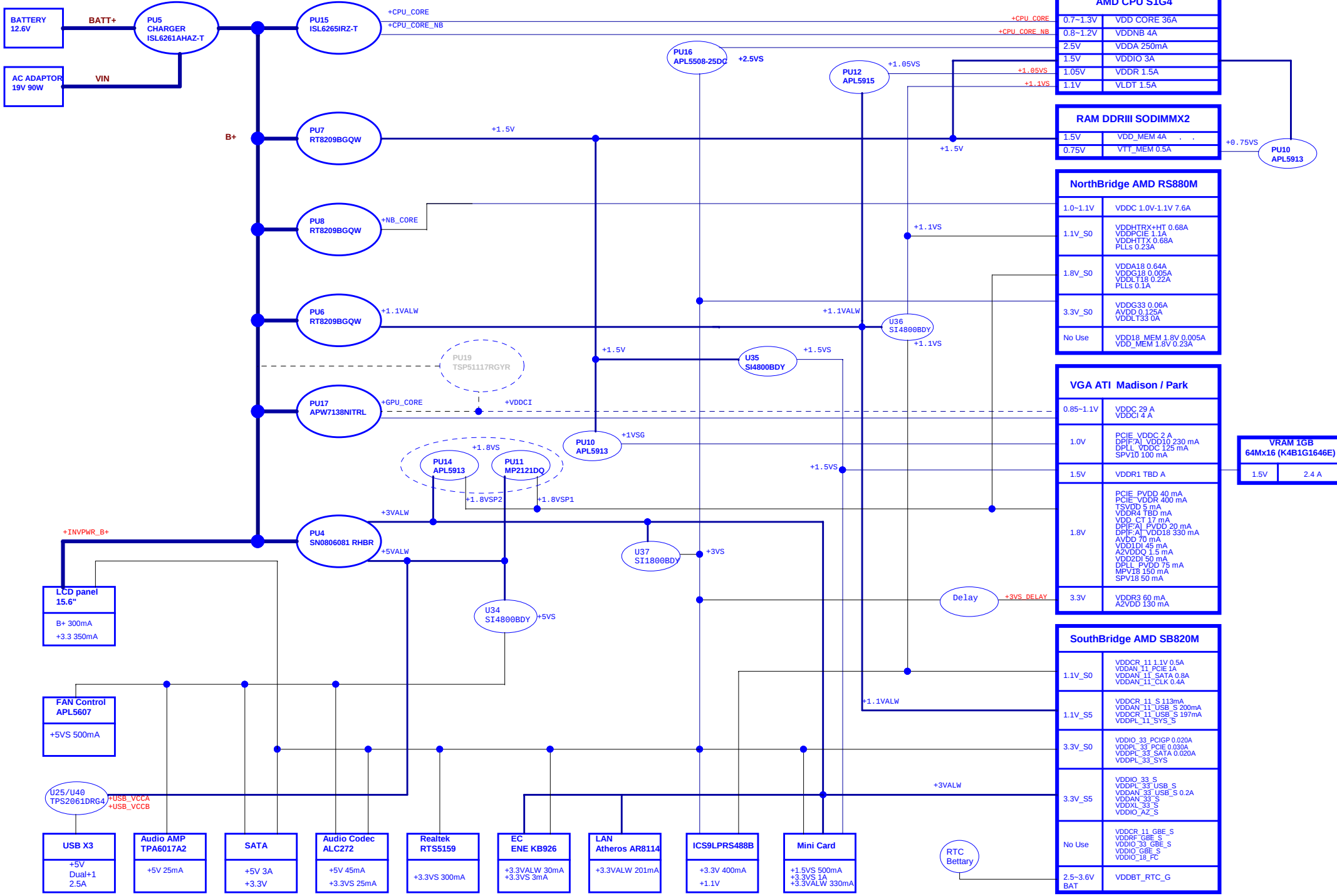
EXT CLKGEN

PowerXpress SKU(Madison): 3G@/BT@/UMA@/ VGA@/SG@/EXT@/EXTPW@/VB@/MAD@
 PowerXpress SKU(Park): 3G@/BT@/UMA@/ VGA@/SG@/EXT@/EXTPW@/VB@/PARK@
 DIS ONLY:(Park) 3G@/BT@/DISO@/ VGA@/EXT@/EXTPW@/PARK@
 UMA only SKU: 3G@/BT@/UMA@/ UMAO@/EXT@/VB@

INT CLKGEN

PowerXpress SKU(Madison):3G@/BT@/UMA@/VGA@/SG@/INT@/VB@/MAD@
 PowerXpress SKU(Park): 3G@/BT@/UMA@/VGA@/SG@/INT@/VB@/PARK@
 DIS ONLY(PARK): 3G@/BT@/DISO@/VGA@/INT@/PARK@
 UMA only SKU: 3G@/BT@/UMA@/UMAO@/INT@/VB@

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				Size B	Document Number	Rev 0.1
				NEW75 LA-5911P		
Date:		Monday, March 22, 2010		Sheet	4 of 55	



AMD CPU S1G4	
0.7~1.3V	VDD CORE 36A
0.8~1.2V	VDDNB 4A
2.5V	VDDA 250mA
1.5V	VDDIO 3A
1.05V	VDDR 1.5A
1.1V	VLDI 1.5A

RAM DDRIII SODIMMx2	
1.5V	VDD_MEM 4A
0.75V	VTT_MEM 0.5A

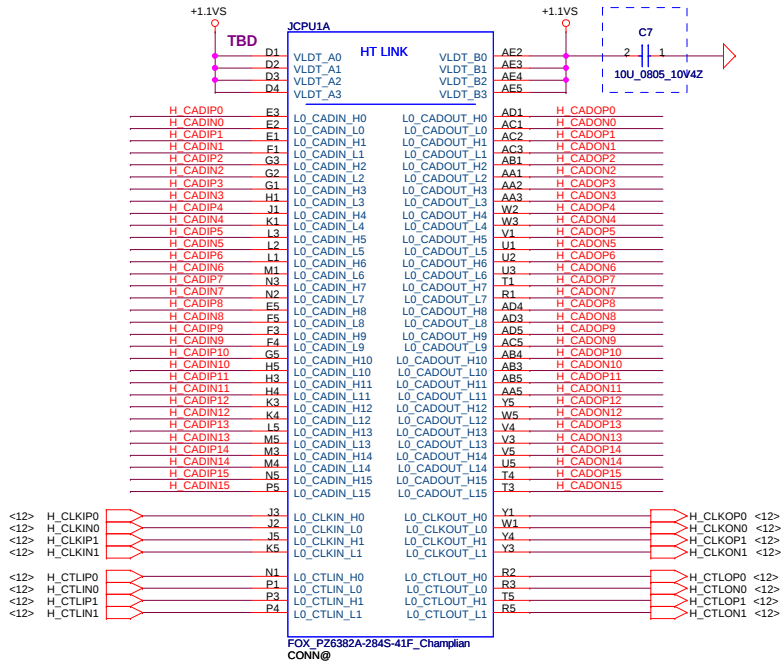
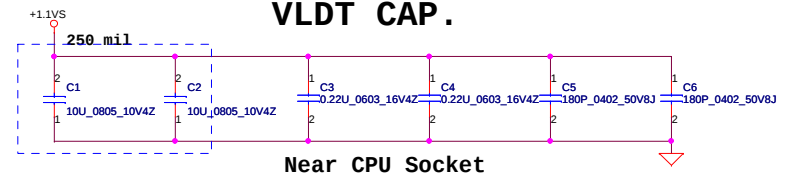
NorthBridge AMD RS880M	
1.0~1.1V	VDDC 1.0V~1.1V 7.6A
1.1V_S0	VDDHTRX+HT 0.68A VDDPCIE 1.1A VDDHTTX 0.68A PLLs 0.23A
1.8V_S0	VDDA18 0.64A VDDG18 0.095A VDDL18 0.22A PLLs 0.1A
3.3V_S0	VDDG33 0.06A AVDD 0.125A VDDL33 0A
No Use	VDD18_MEM 1.8V 0.005A VDD_MEM 1.8V 0.23A

VGA ATI Madison / Park	
0.85~1.1V	VDDC 29 A VDDCI 4 A
1.0V	PCIE_VDDC 2 A DP1F_A VDD10 230 mA DPLL_VDDC 125 mA SPV10 100 mA
1.5V	VDDR1 TBD A
1.8V	PCIE_PVDD 40 mA PCIE_VDDR 400 mA TSVDD 5 mA VDDR4 TBD mA VDD_CT 17 mA DP1F_A PVDD 20 mA DP1F_A VDD18 330 mA AVDD 70 mA VDD1D1 45 mA AZVDDQ 1.5 mA VDD2D1 50 mA DPLL_PVDD 75 mA MPV18 150 mA SPV18 50 mA
3.3V	VDDR3 60 mA A2VDD 130 mA

VRAM 1GB 64Mx16 (K4B1G1646E) * 8	
1.5V	2.4 A

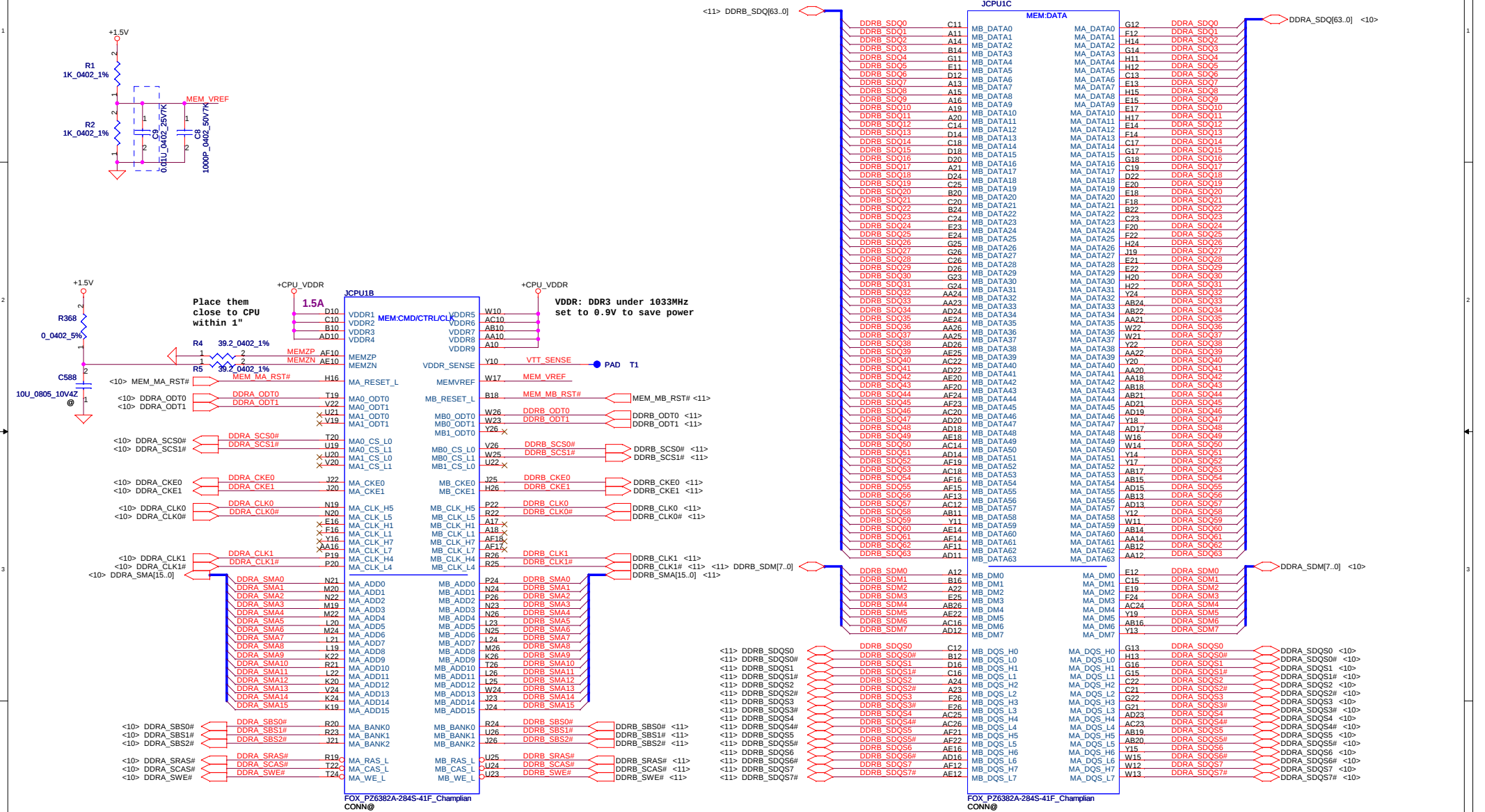
SouthBridge AMD SB820M	
1.1V_S0	VDDCR_11 1.1V 0.5A VDDAN_11 PCIE 1A VDDAN_11 SATA 0.8A VDDAN_11_CLK 0.4A
1.1V_S5	VDDCR_11_S 113mA VDDAN_11_USB_S 200mA VDDCR_11_USB_S 197mA VDDL_11_SY_S
3.3V_S0	VDDIO_33 PCIGP 0.020A VDDL_33 PCIE 0.030A VDDL_33 SATA 0.020A VDDL_33_SY_S
3.3V_S5	VDDIO_33_S VDDL_33_USB_S VDDAN_33_S VDDL_33_S VDDL_33_S VDDIO_AZ_S
No Use	VDDCR_11_GBE_S VDDR_F_GBE_S VDDIO_33_GBE_S VDDIO_38_FC VDDIO_38_FC
2.5~3.6V BAT	VDDBT_RTC_G

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<12> H_CADIN[0..15] H_CADIN[0..15] <12>

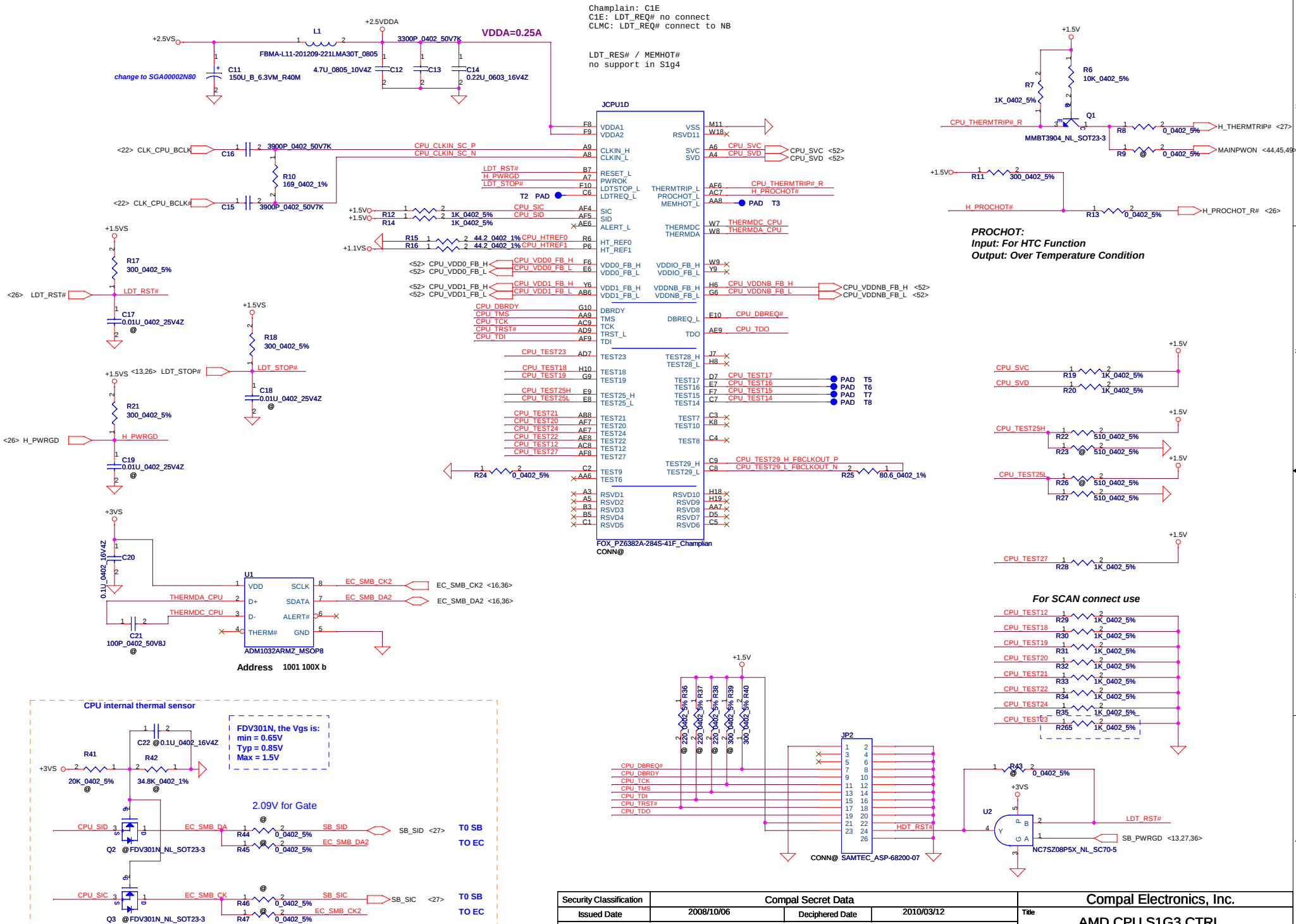


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										Rev 0.1	
										Date: Monday, March 22, 2010	
										Sheet 6 of 55	

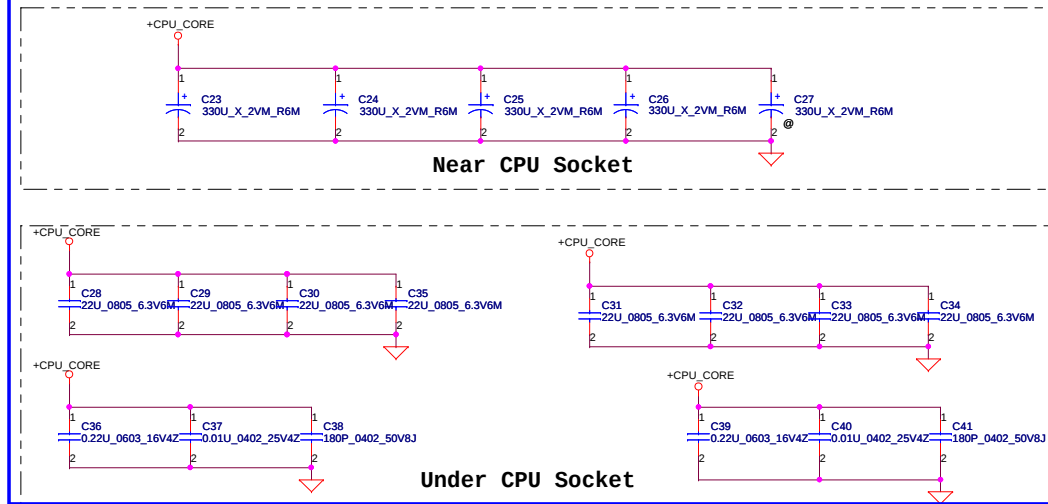
Processor DDR3 Memory Interface



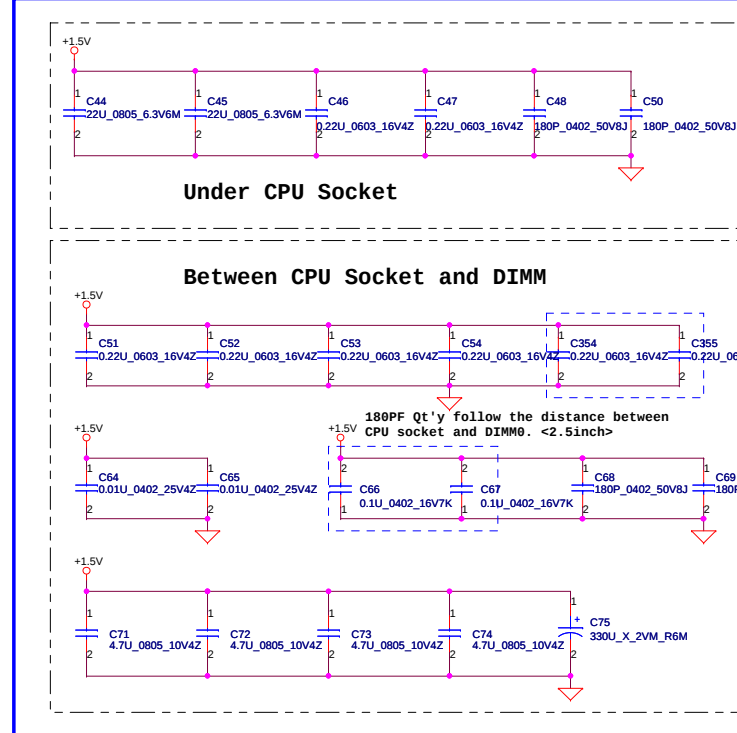
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		Size	Document Number						Rev
		Custom	NEW75 LA-5911P						0.1
		Date:	Monday, March 22, 2010			Sheet	7	of	55



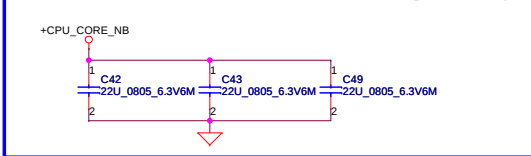
VDD(+CPU_CORE) decoupling.



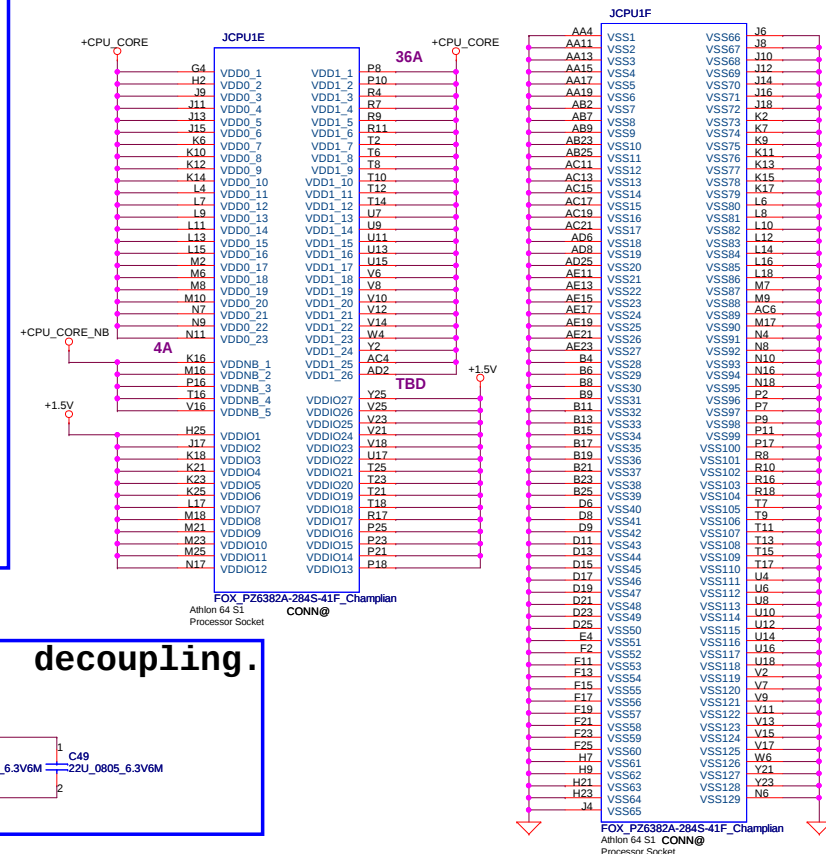
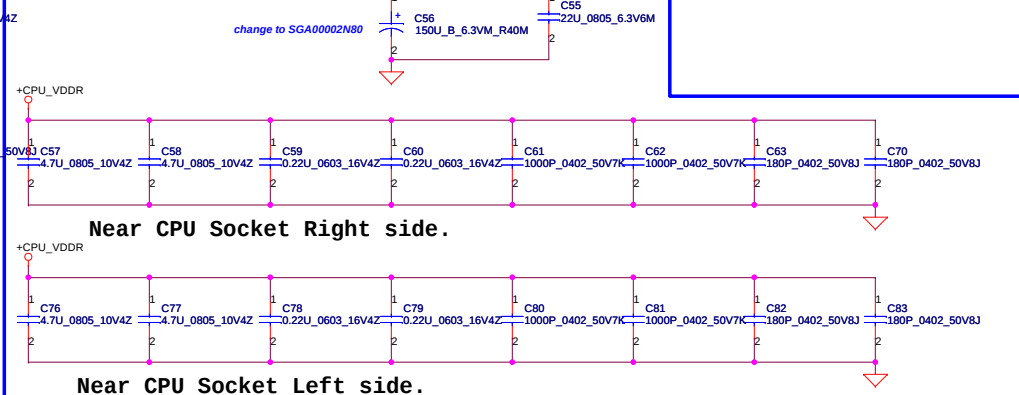
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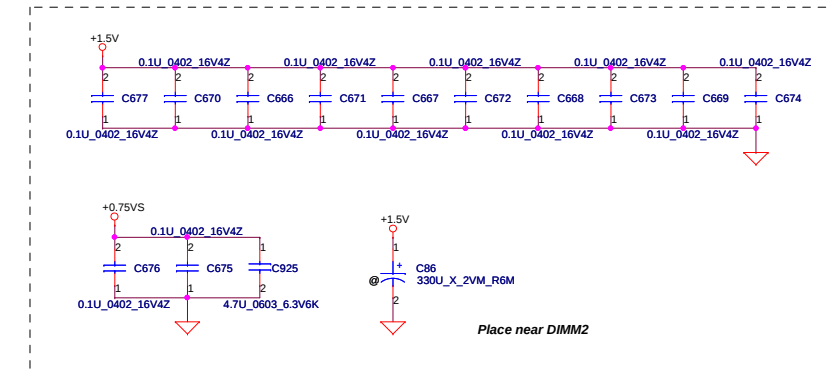
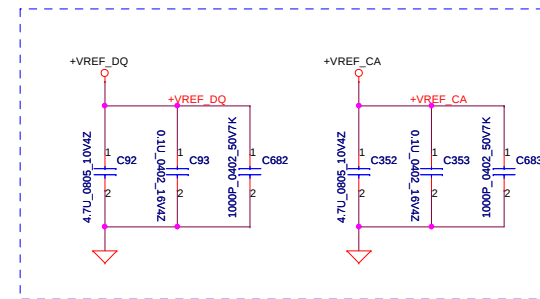
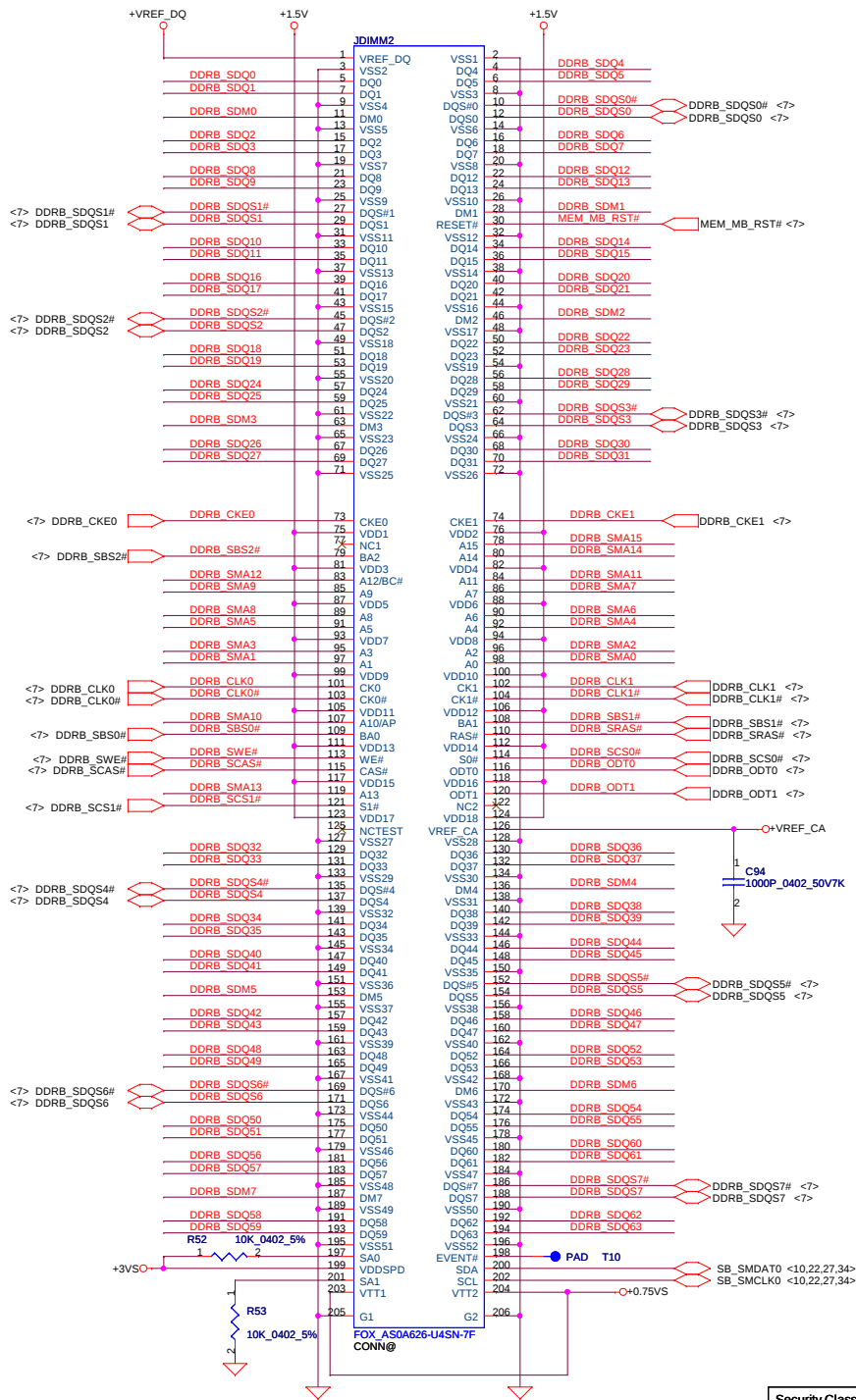


+CPU_CORE_NB decoupling.



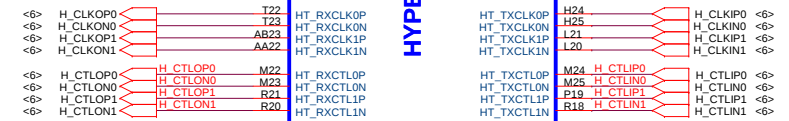
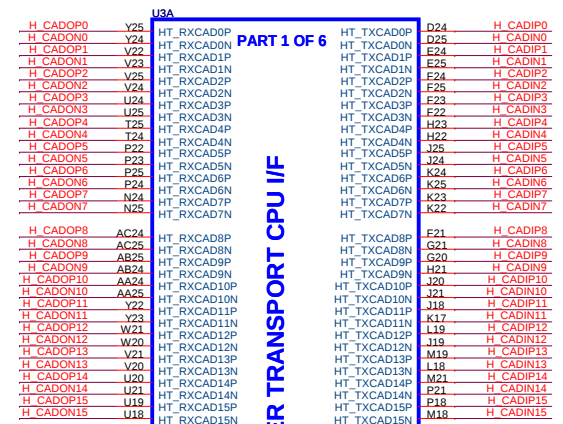
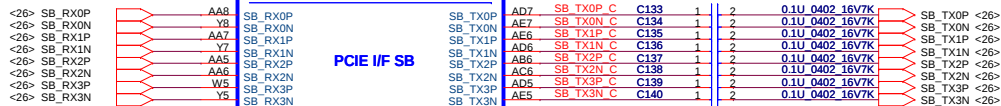
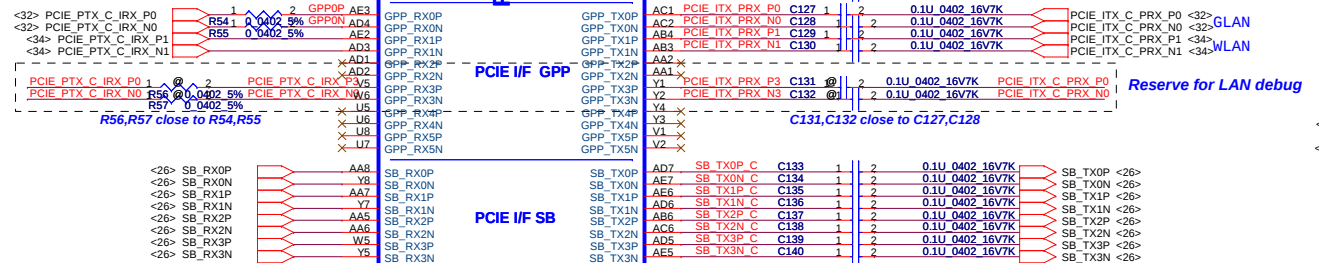
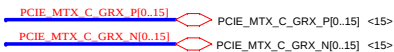
VDDR decoupling.

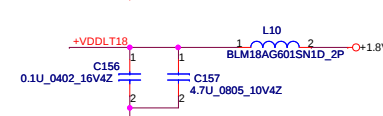
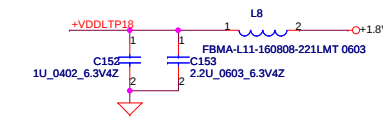
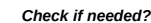
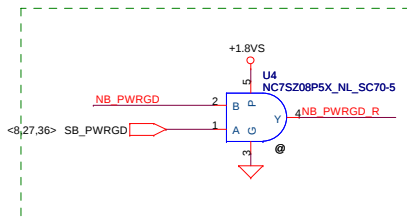
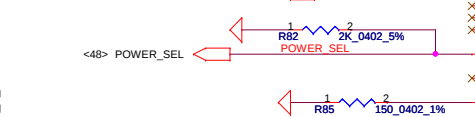
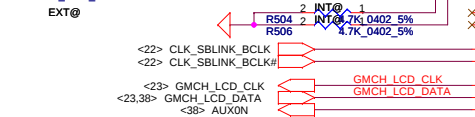
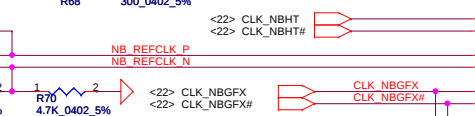
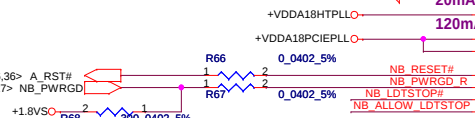
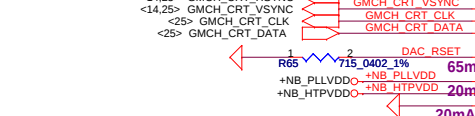
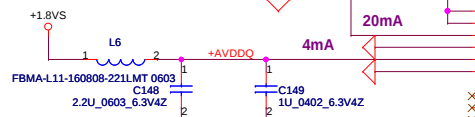
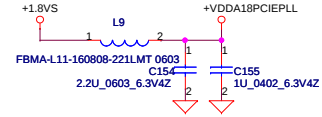




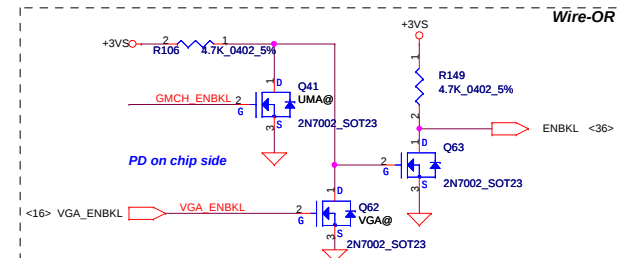
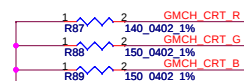
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Size	Document Number	Rev		NEW75 LA-5911P	
Date:	Monday, March 22, 2010	Sheet	11	of 55	

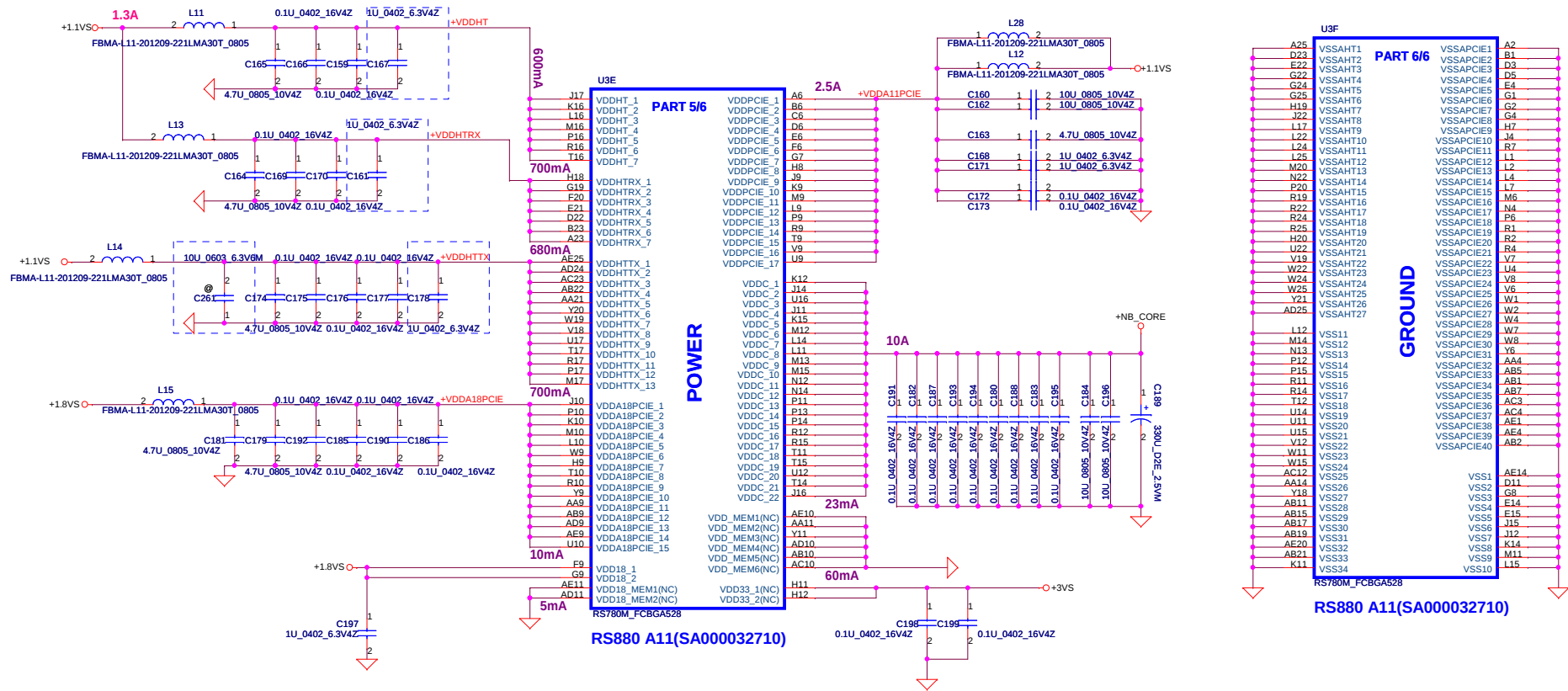




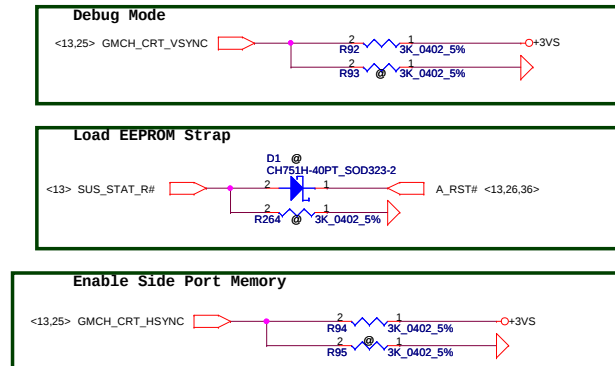
RS880	POWER_SEL
HIGH	0.95V
LOW	1.1V



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				Size	Rev
				Custom	0.1
NEW75 LA-5911P				Date: Monday, March 22, 2010	
[Sheet 13 of 55]				[Sheet 13 of 55]	



Side port and Strap setting



DFT GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEB

Enables the Test Debug Bus using GPIO. (VSYNC)

1 : Disable
0 : Enable

DFT GPIO1: LOAD_EEPROM_STRAPS

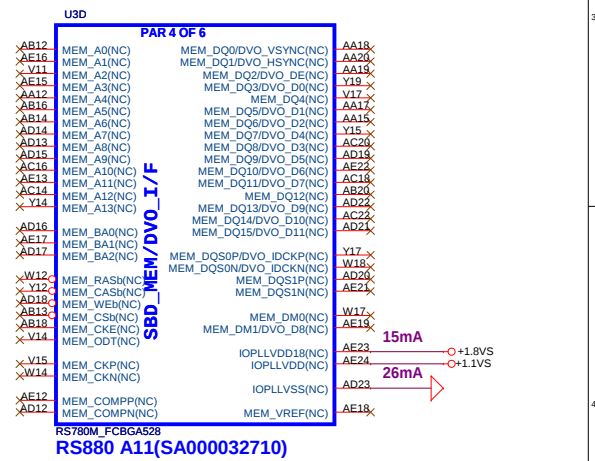
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : T2C Master can load strap values from EEPROM if connected, or use default values if not connected

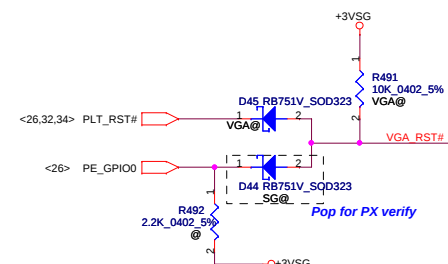
Enable Side Port Memory

RS880: HSYNC#
0: Enable
1: Disable

Register Readback of strap:
NB_CLKCFG:CLK_TOP_SPARE_D[1]

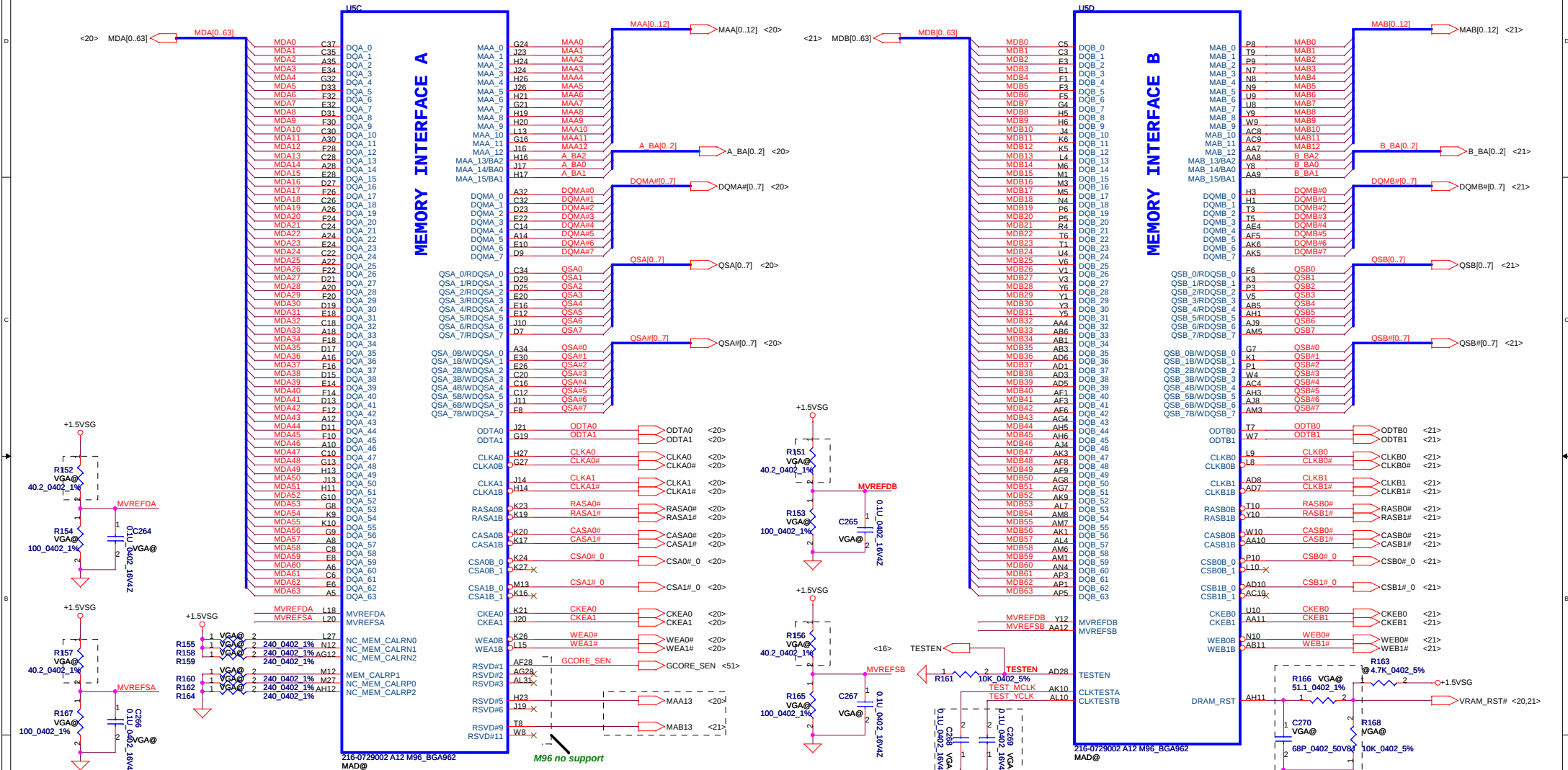


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				Size	Document Number	Rev
				Cust	NEW75 LA-5911P	0.1
Date: Monday, March 22, 2010		Sheet 14 of 55				



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				Cust	NEW75 LA-5911P	0.
				Date:	Monday, March 22, 2010	Sheet 15 of 55

Park only support single channel memory (channel B only)



If use M96 upper resistor will change to 100ohm for MVREFDA/B and MVREFSA/B
Mahatten upper resistor use 40.2ohm

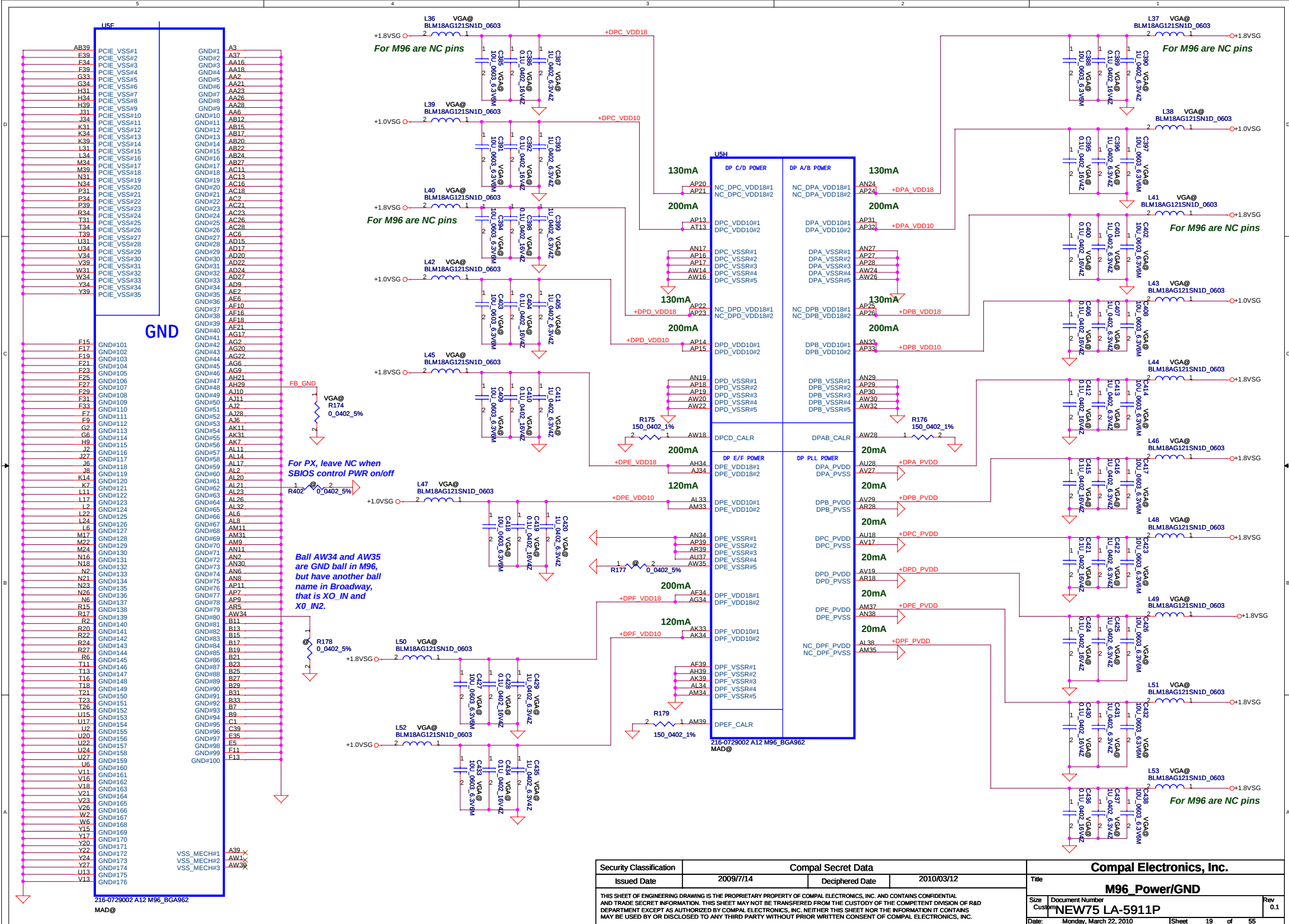
In M97, Medison and Park, AF28 is FB_VDDC, AG28 is FB_VDDCI, AH29 is FB_GND. GCORE_SEN and FB_GND should route as differential pair Same as VDDCI_SEN and FB_GND

If use M96 upper resistor will change to 100ohm for MVREFDA/B and MVREFSA/B
Mahatten upper resistor use 40.2ohm

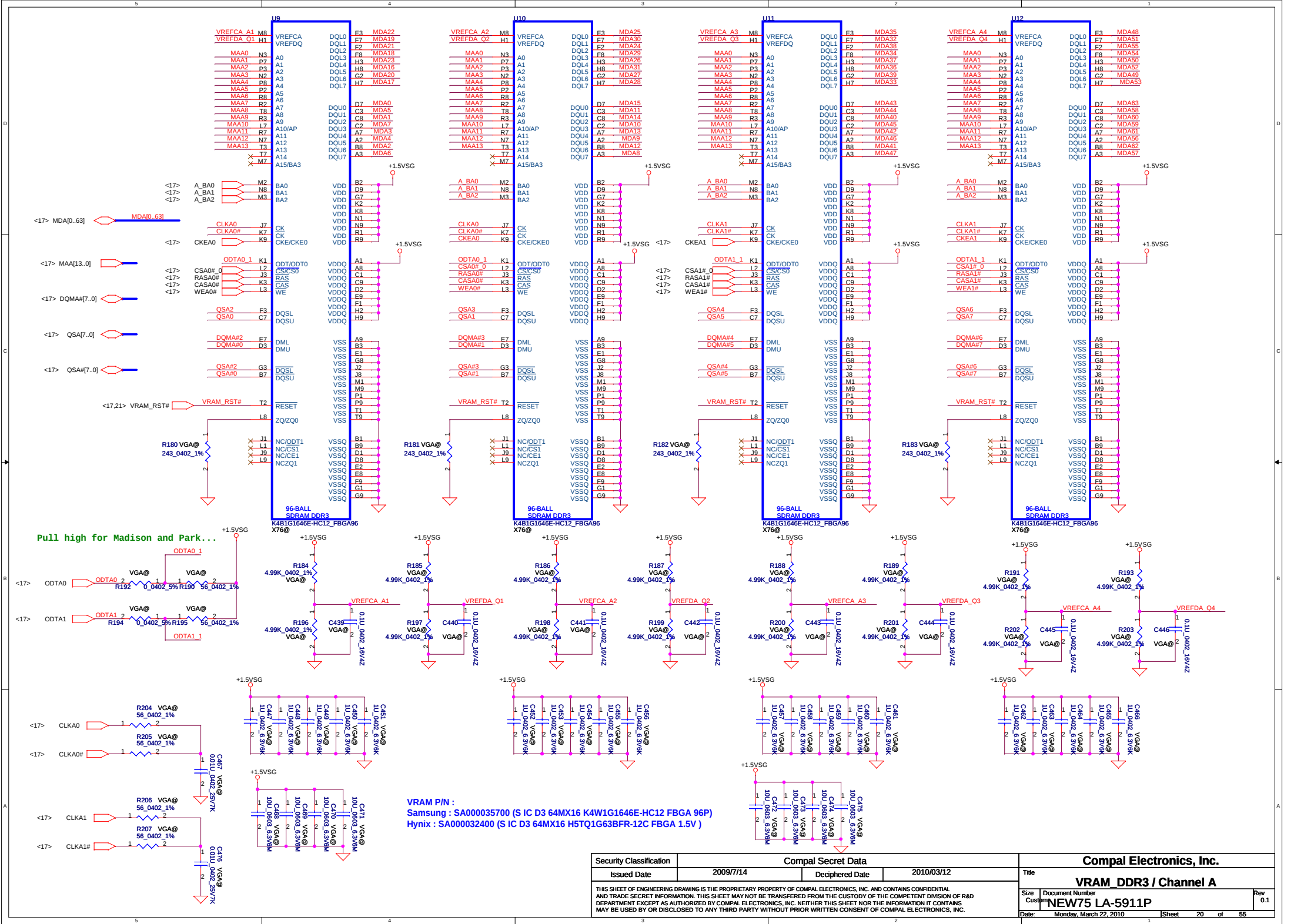
M96 use 4.7K to PD directly.

	M96	Broadway
R168	4.7k Ohm SD028470180	10k Ohm SD028100280
R166	0 Ohm SD028000000	680 Ohm SD028680000
R163	4.7k Ohm SD028470180	DNI
C276	1000 pF SF074102K00	68 pF SF071600180

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					NEW75 LA-5911P	0.1
				Date:	Monday, March 22, 2010	Sheet 17 of 55

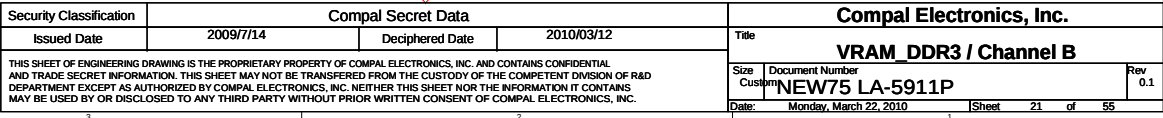


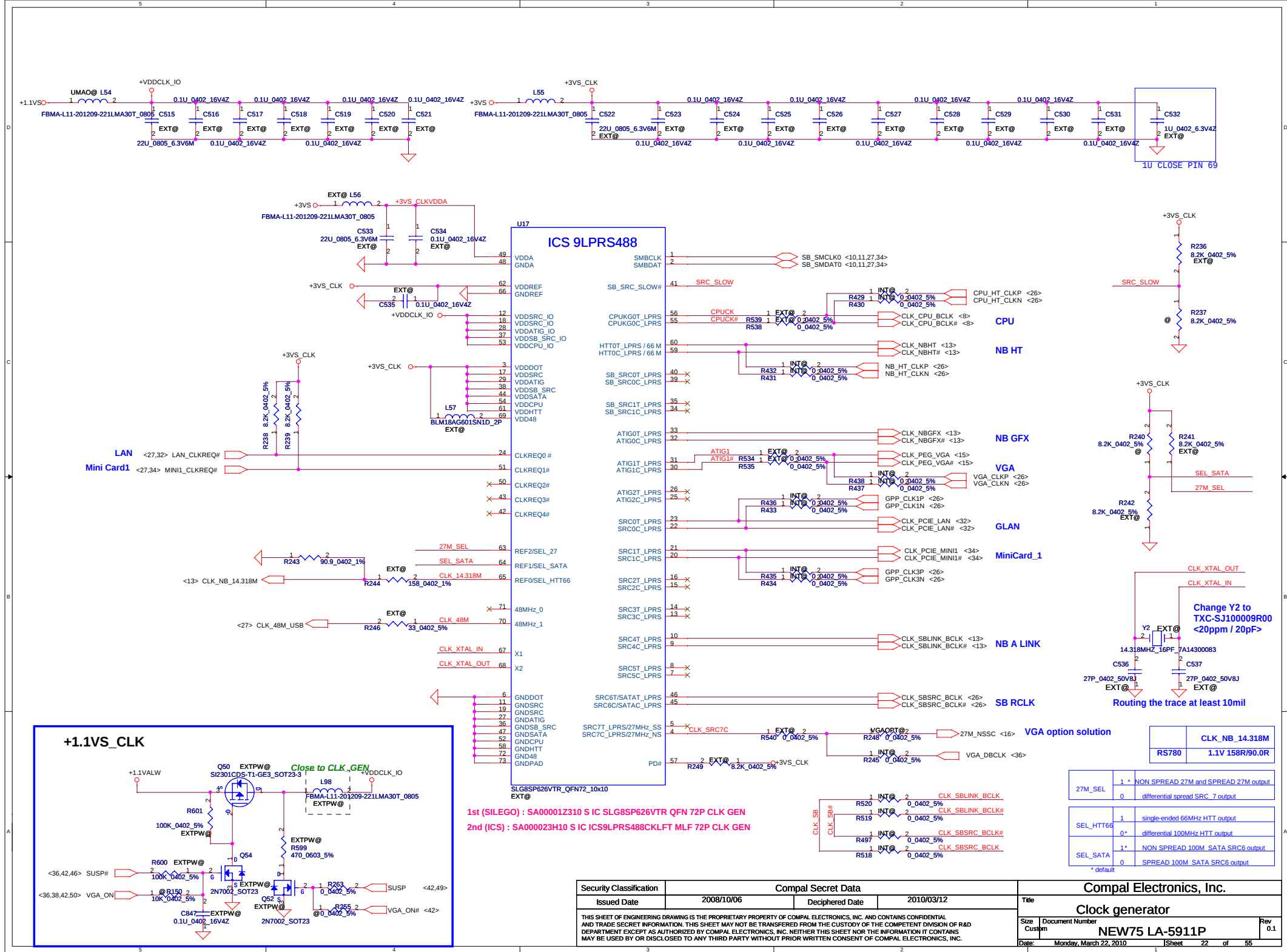
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2009/7/14	Deciphered Date	2010/03/12	Title M96_Power/GND		
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					NEW75 LA-5911P	0.1
Date:				Monday, March 22, 2010	Sheet	19 of 55



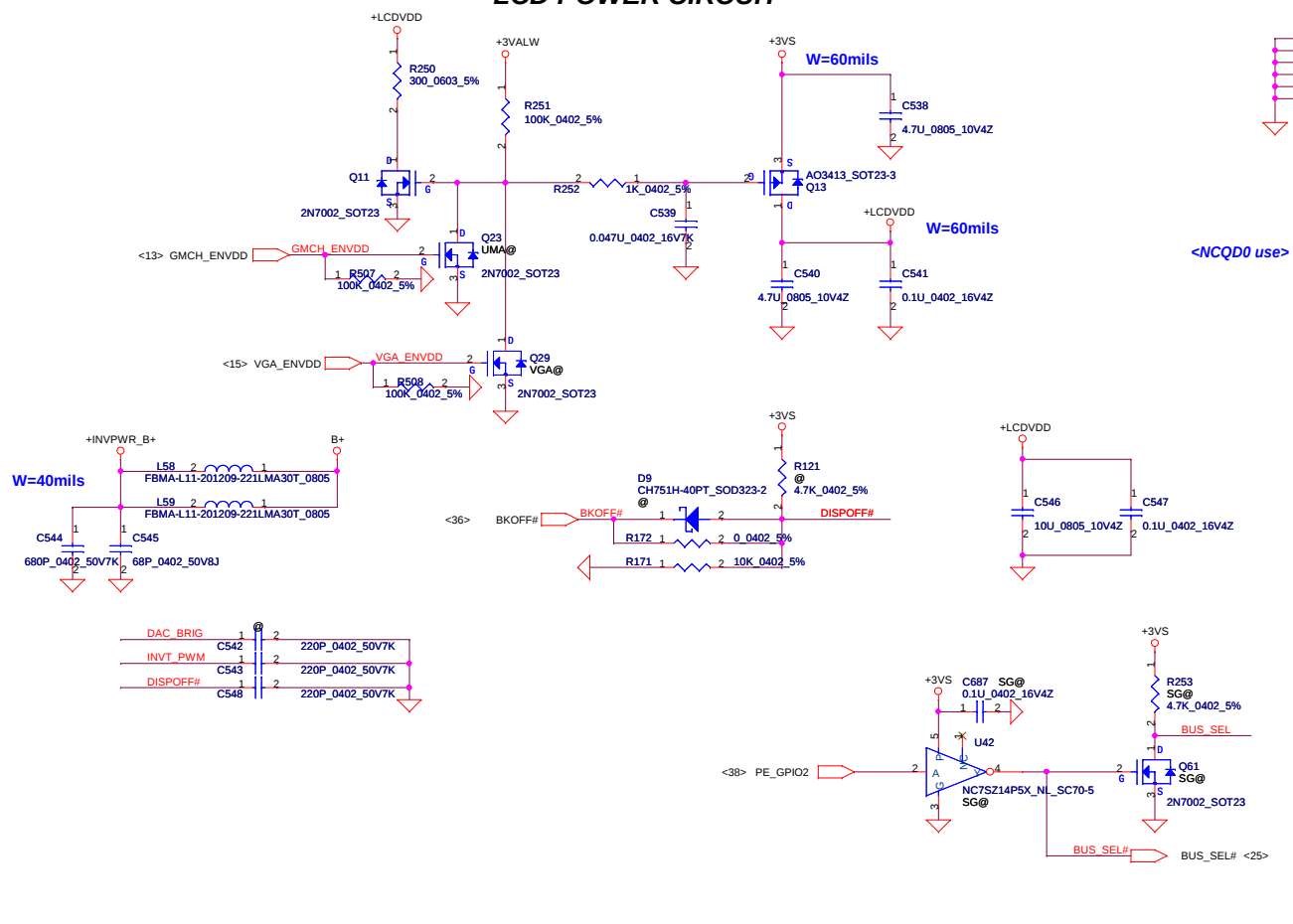
VRAM P/N :
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

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								Size		Document Number		Rev	
								Customer		NEW75 LA-5911P		0.1	
								Date		Monday, March 22, 2010		Sheet 20 of 55	

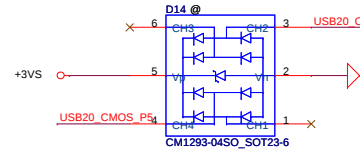
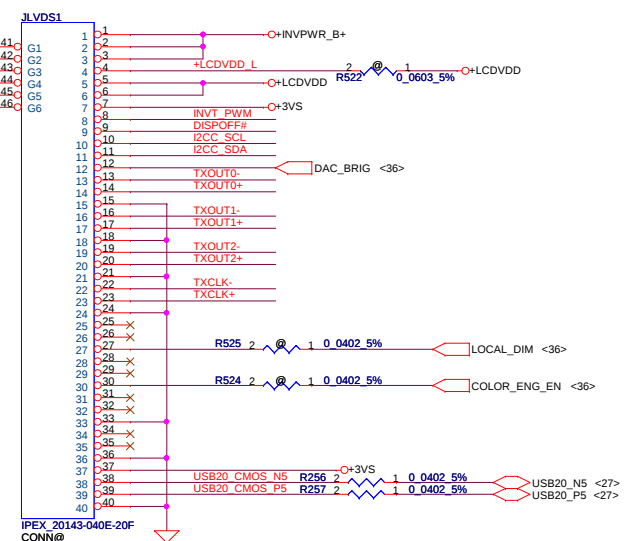




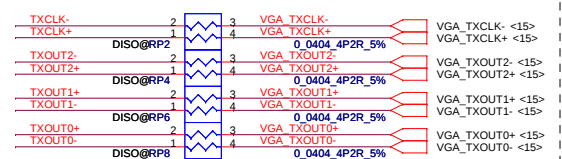
LCD POWER CIRCUIT



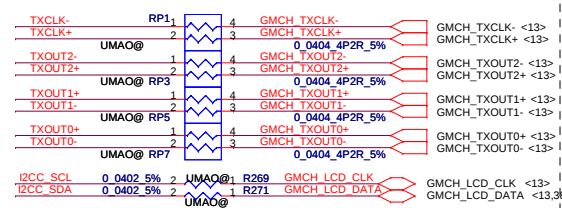
LCD/LED PANEL Conn.



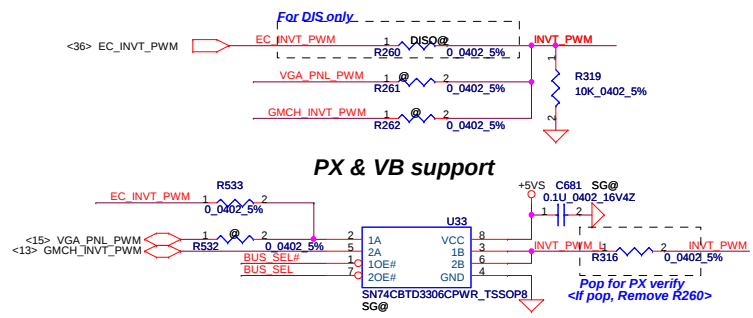
VGA ONLY



UMA ONLY

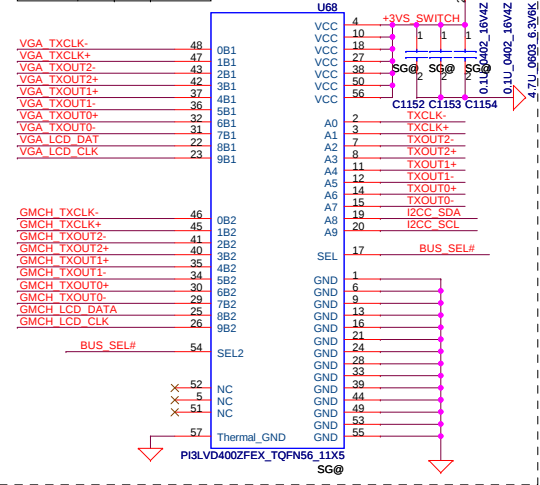


PX & VB support

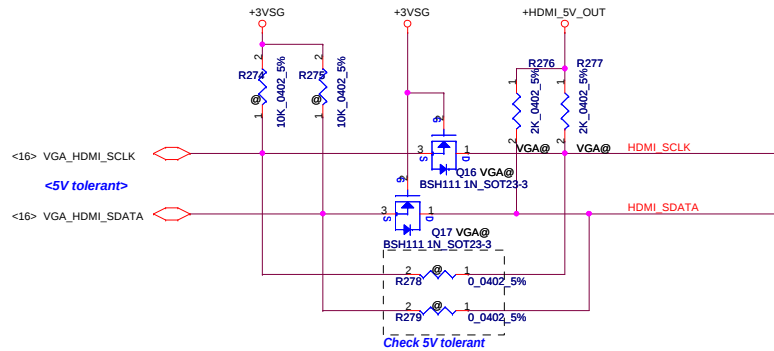


1OE#	L	B1	DIS
	H	Z	
2OE#	L	B1	UMA
	H	Z	

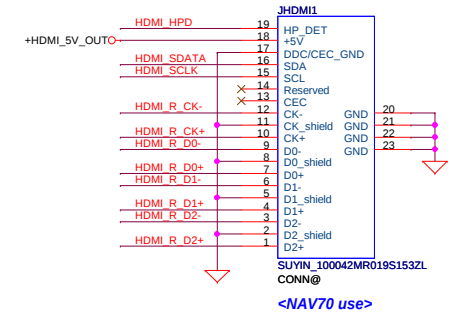
SEL1	L	B1	DIS
<BUS>	H	B2	UMA
SEL2	L	B1	DIS
<DCC>	H	B2	UMA



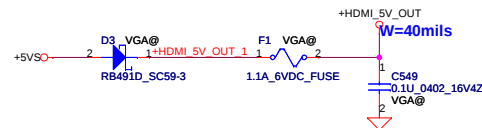
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				Date: Monday, March 22, 2010	Sheet 23 of 55



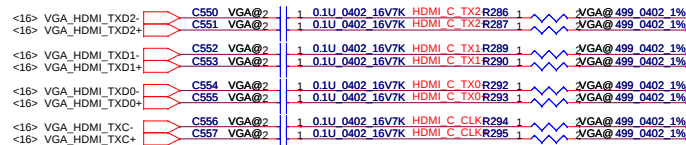
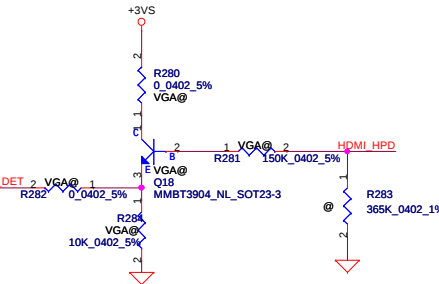
Place closed to JHDMI1



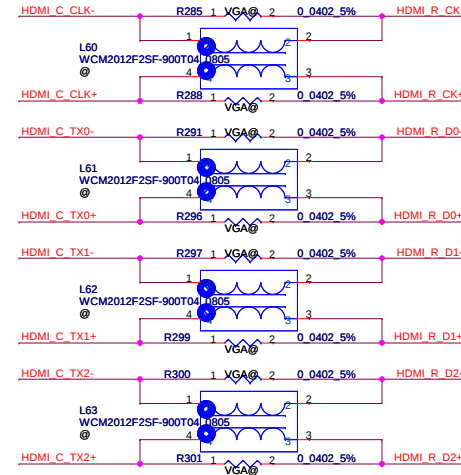
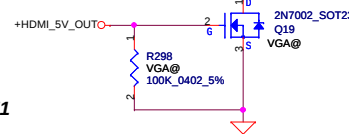
<NAV70 use>



<16.27> VGA_HDMI_DET



Place closed to JHDMI1

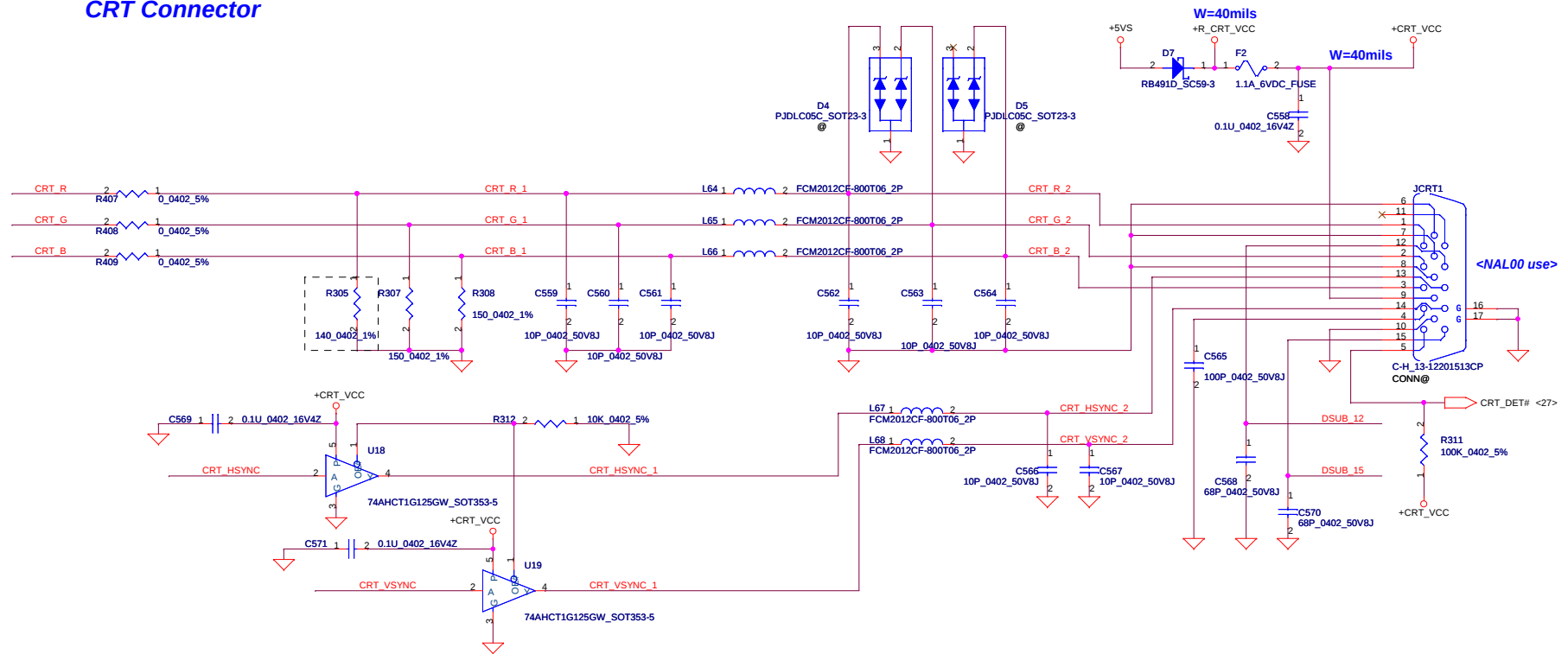


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				Deciphered Date				HDMI Connector			
				2010/03/12				Size			
								Document Number			
								NEW75 LA-5911P			
								Date			
								Monday, March 22, 2010			
								Sheet			
								24 of 55			

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Rev 0.1

CRT Connector

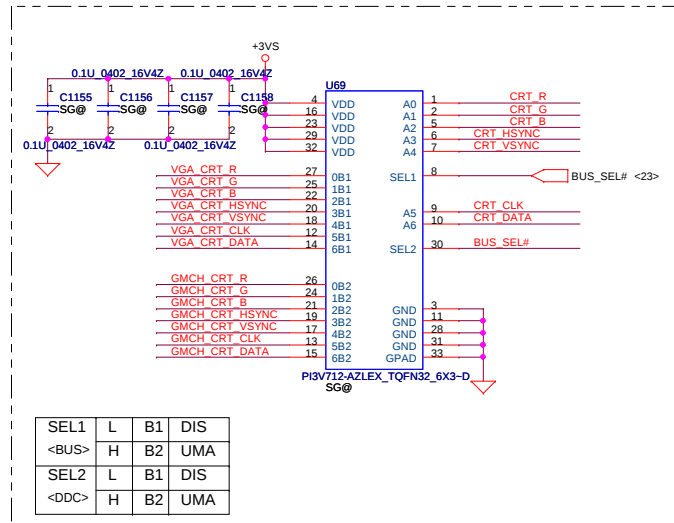


For UMA Only

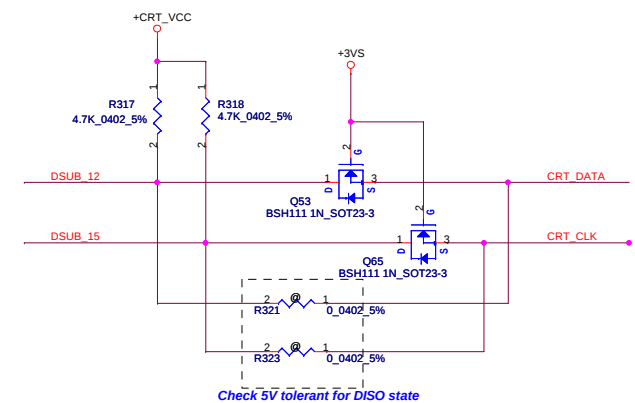
Component	Signal	Value	Unit	Frequency	Phase	Signal
<13> GMCH_CRT_R	GMCH CRT R	R266	2	UMAC0	0.0402 5%	CRT R
	GMCH CRT G	R83	2	UMAC0	0.0402 5%	CRT G
<13> GMCH_CRT_G	GMCH CRT B	R268	2	UMAC0	0.0402 5%	CRT B
	GMCH CRT_B					
<13,14> GMCH_CRT_HSYNC	GMCH CRT_HSYNC	R273	2	UMAC0	0.0402 5%	CRT_HSYNC
	GMCH CRT_VSYNC	R267	2	UMAC0	0.0402 5%	CRT_VSYNC
<13,14> GMCH_CRT_VSYNC	GMCH CRT_DATA	R410	2	UMAC0	0.0402 5%	CRT DATA
	GMCH CRT_CLK	R406	2	UMAC0	0.0402 5%	CRT_CLK

For VGA Only

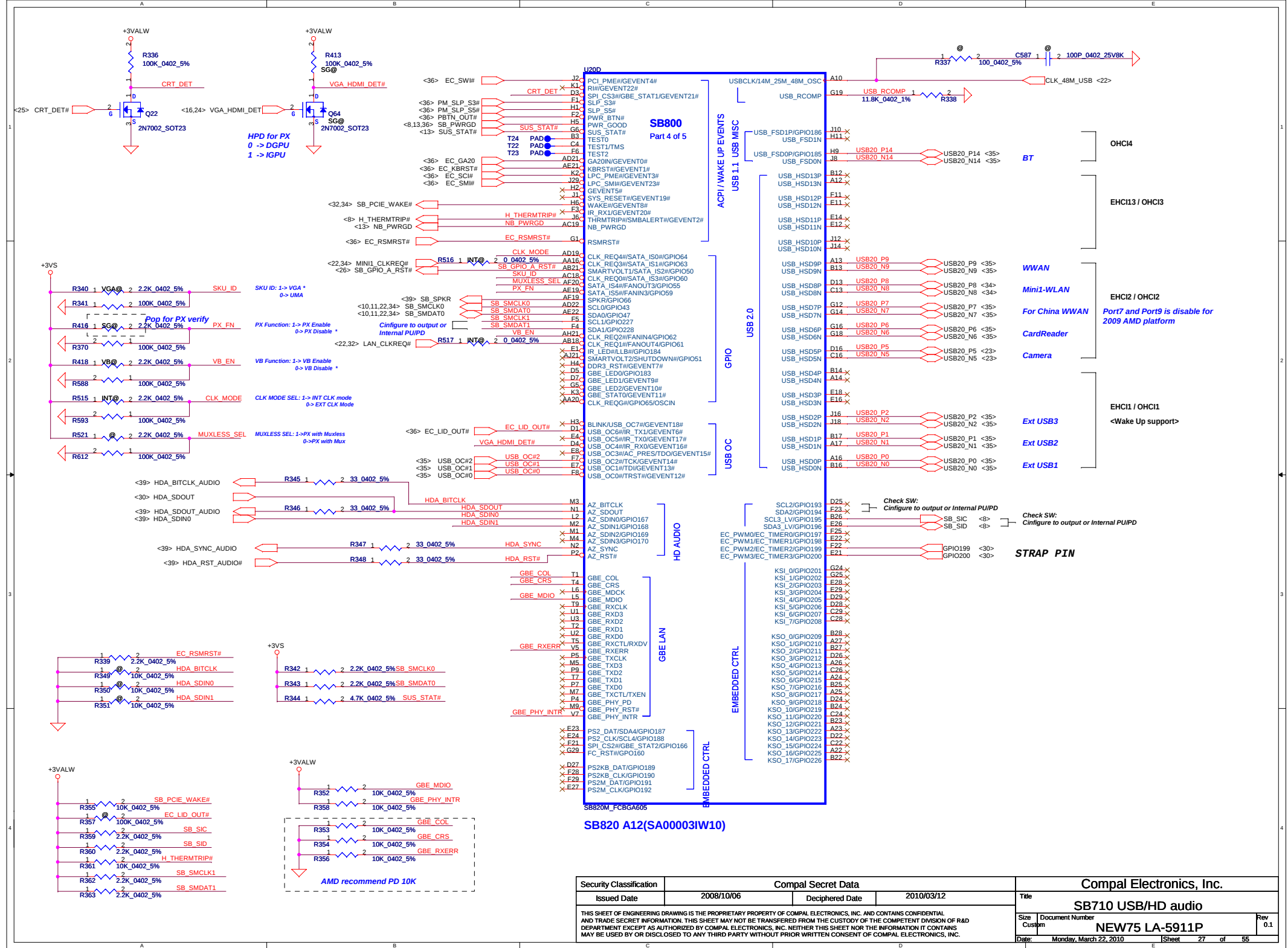
Device	Signal	Pin	Package	IO Standard	IO Voltage	IO Current	IO Power	IO Type
<16>	VGA_CRT_R	VGA CRT_R	R306	DSOC	1	0	0.0402 5%	CRT_R
<16>	VGA_CRT_G	VGA CRT_G	R302	DSOC	1	0	0.0402 5%	CRT_G
<16>	VGA_CRT_B	VGA CRT_B	R304	DSOC	1	0	0.0402 5%	CRT_B
<16>	VGA_CRT_HSYNC	VGA CRT_HSYNC	R303	DSOC	1	0	0.0402 5%	CRT_HSYNC
<16>	VGA_CRT_VSYNC	VGA CRT_VSYNC	R309	DSOC	1	0	0.0402 5%	CRT_VSYNC
<16>	VGA_CRT_DATA	VGA CRT_DATA	R411	DSOC	1	0	0.0402 5%	CRT_DATA
<16>	VGA_CRT_CLK	VGA CRT_CLK	R412	DSOC	1	0	0.0402 5%	CRT_CLK



Close to Conn side

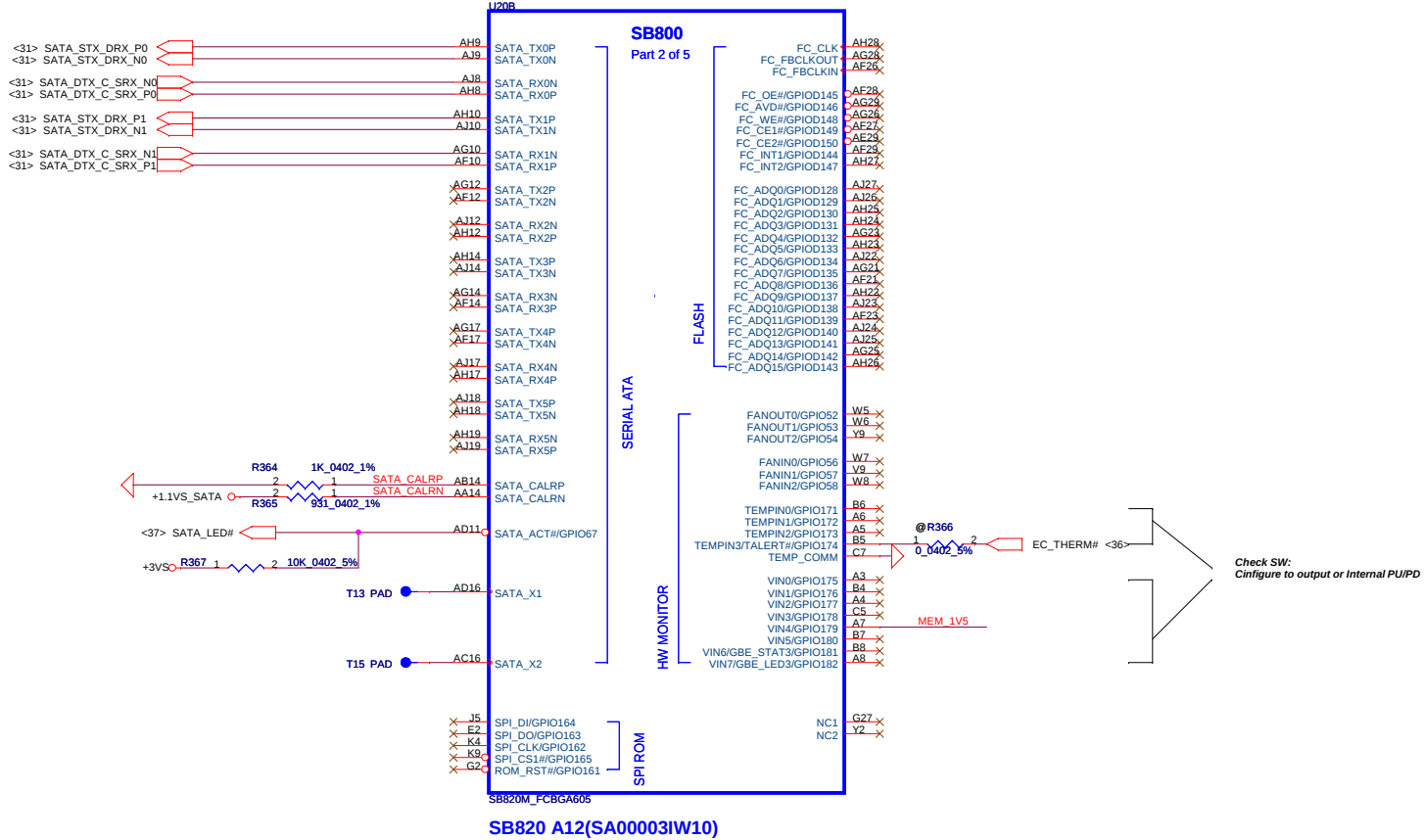


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				NEW75 LA-5911P		
				Date	Monday, March 22, 2010	Sheet 25 of 55

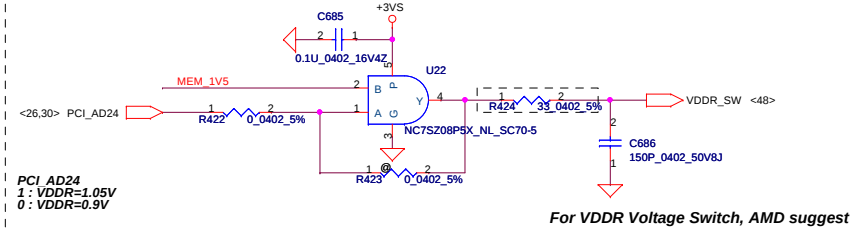


HDD

ODD



MEM_1V5 is for gating the glitch on PCI_AD24

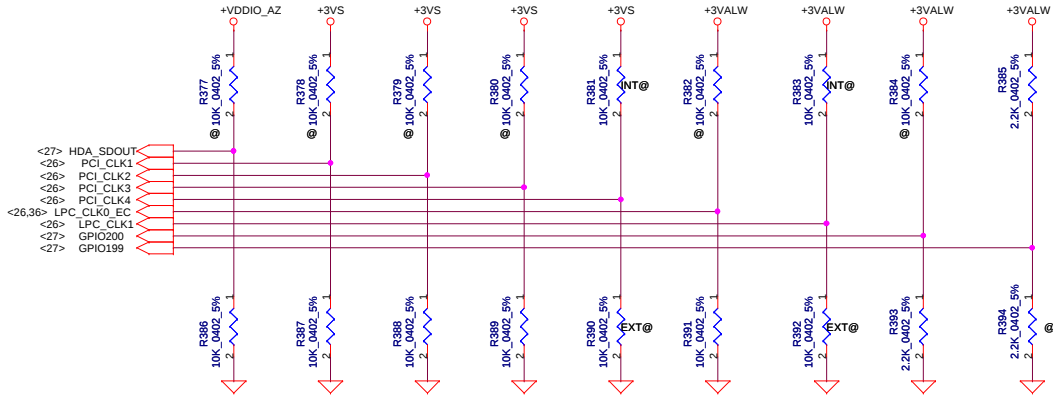


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Size	Document Number	Rev		NEW75 LA-5911P	
Custpm		Date		Monday, March 22, 2010	
		Sheet		28 of 55	

REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	CPU/HT CLK SEL Enable	EC ENABLE	CLOCKGEN ENABLE	H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default L,NC) L,L = FWH ROM	
PULL LOW	Performance MODE	FORCE PCIE GEN1	WATCHDOG TIMER DISABLE	IGNORE DEBUG STRAP	CPU/HT CLK SEL Disable	EC DISABLE	CLOCKGEN DISABLE		
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT		



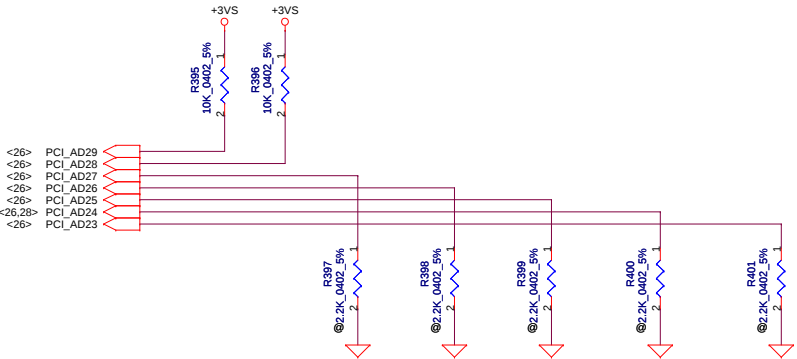
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

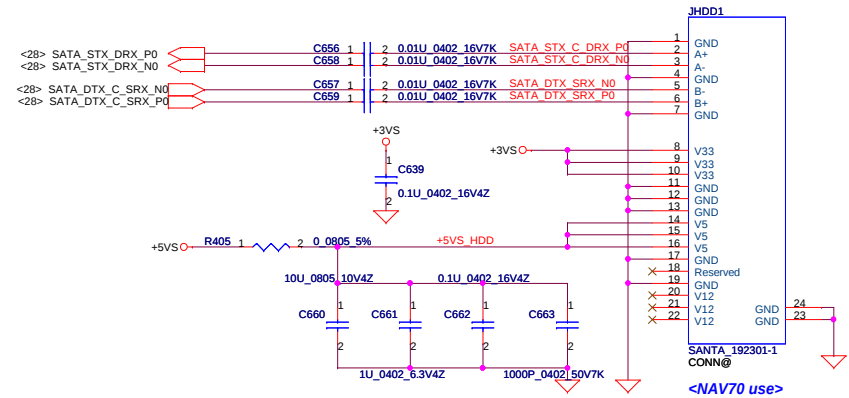
		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH		USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW		BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

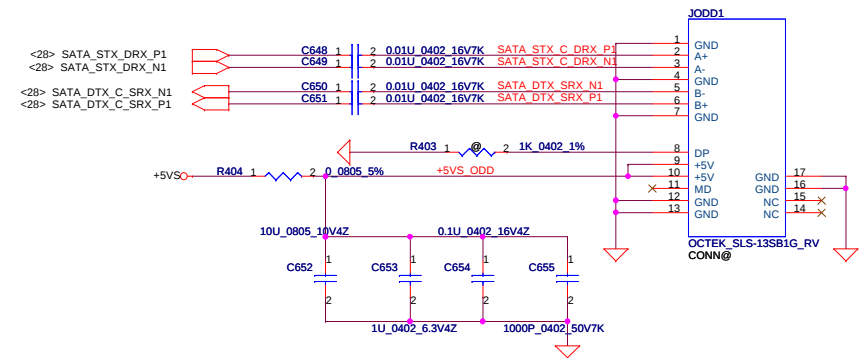
check default

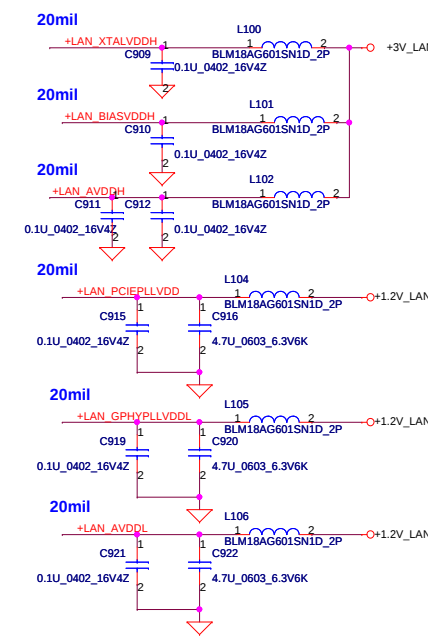


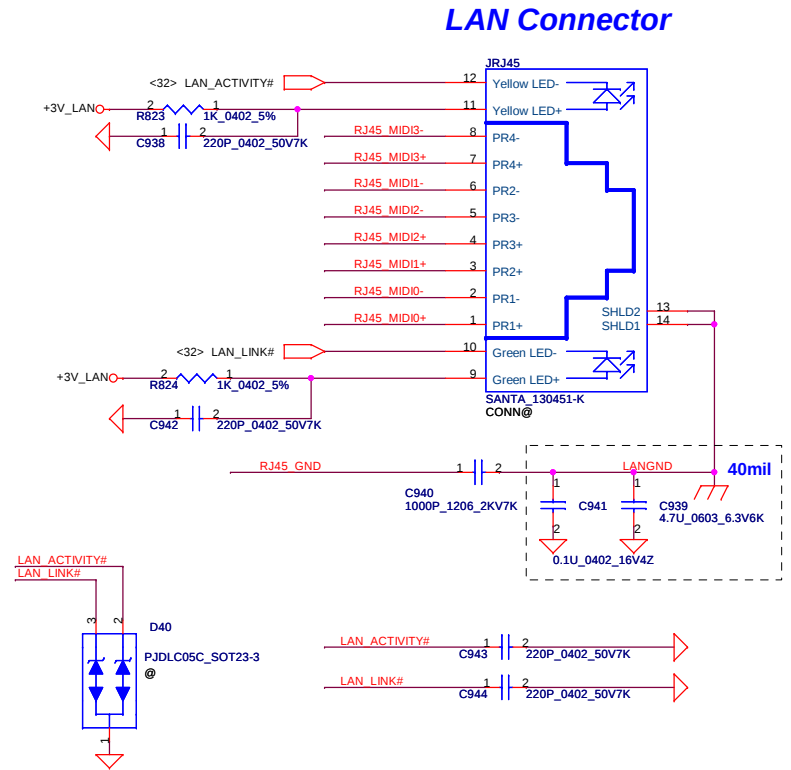
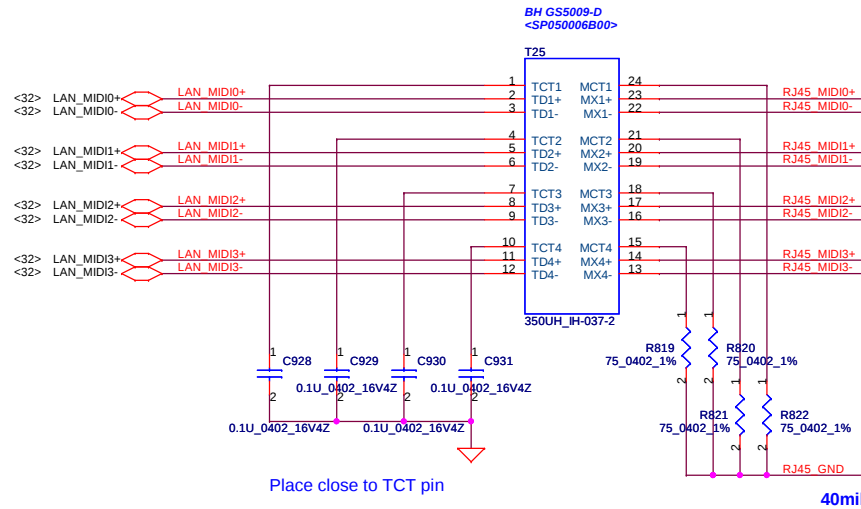
SATA HDD Conn.



SATA ODD Conn.

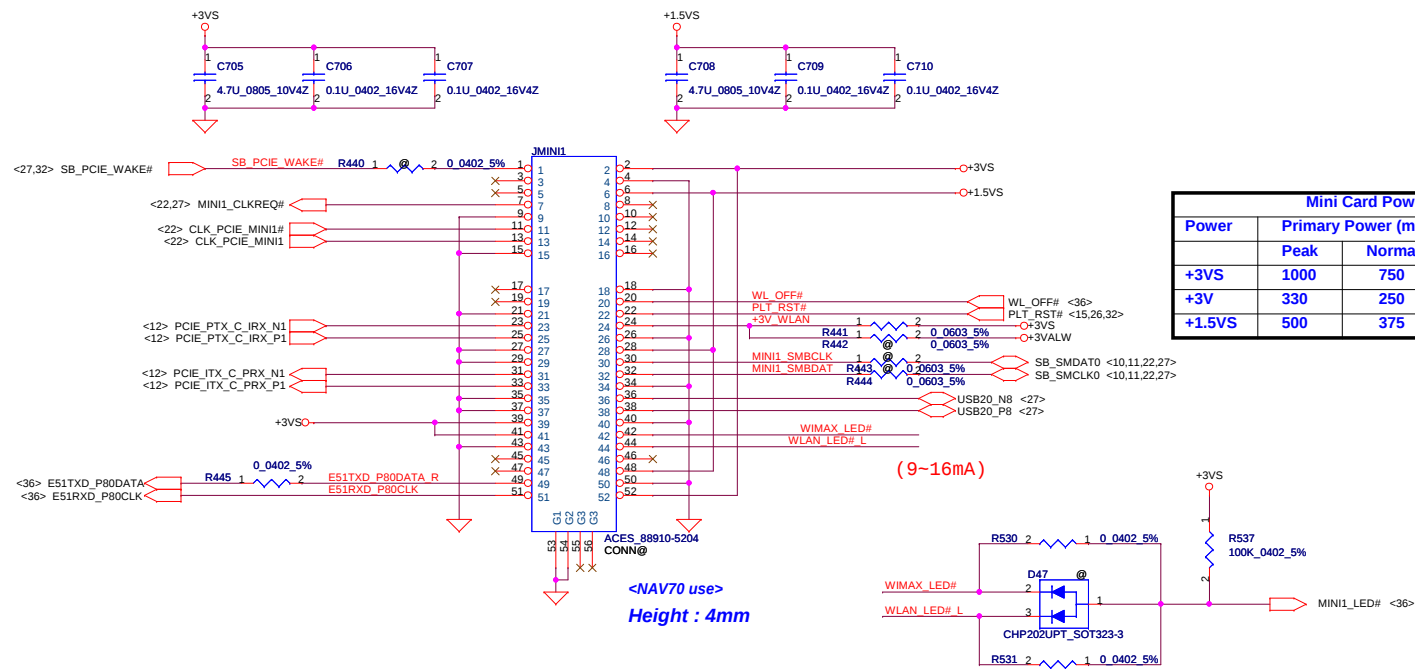




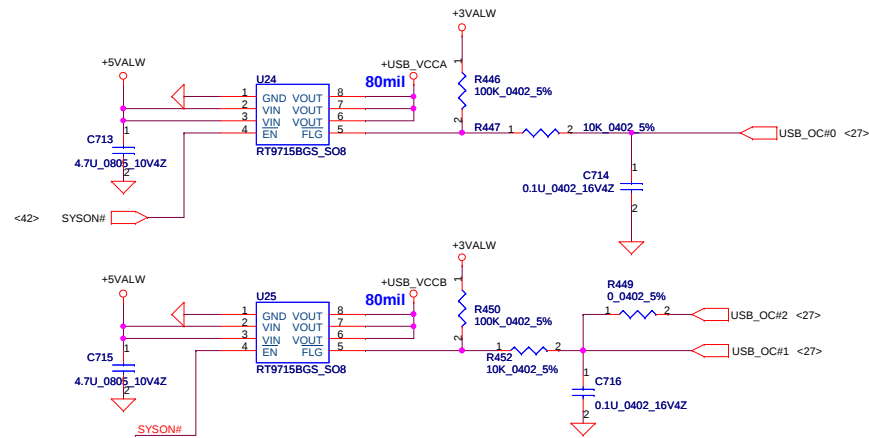


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				NEW75 LA-5911P	
				Date:	Monday, March 22, 2010
				Sheet	33 of 55
				Rev	0.1

Mini-Express Card for WLAN

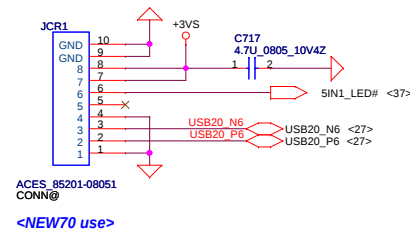
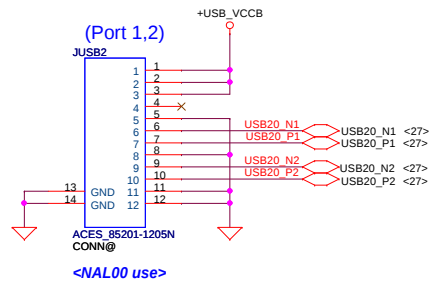
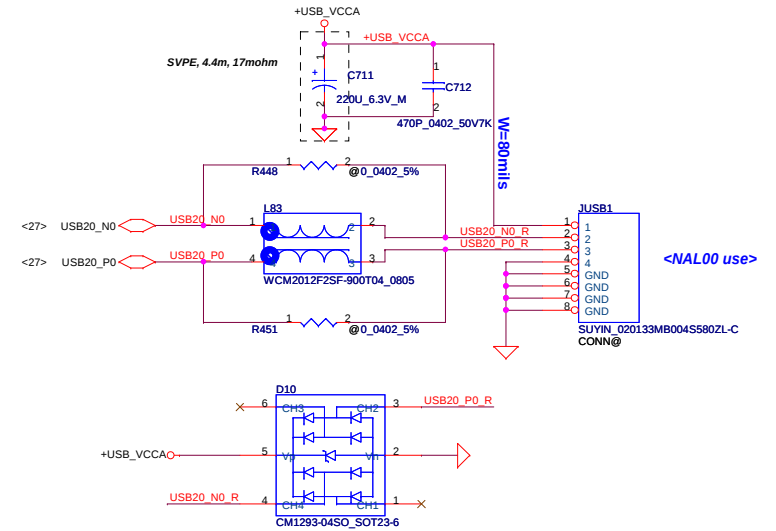


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

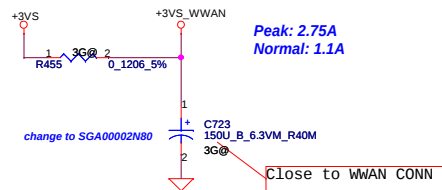
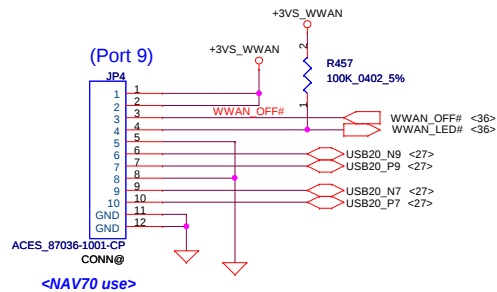


To USB/B Connector

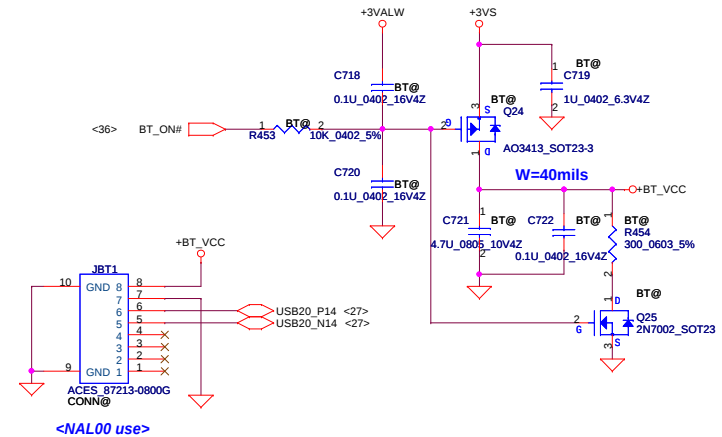
To CardReader/B Connector



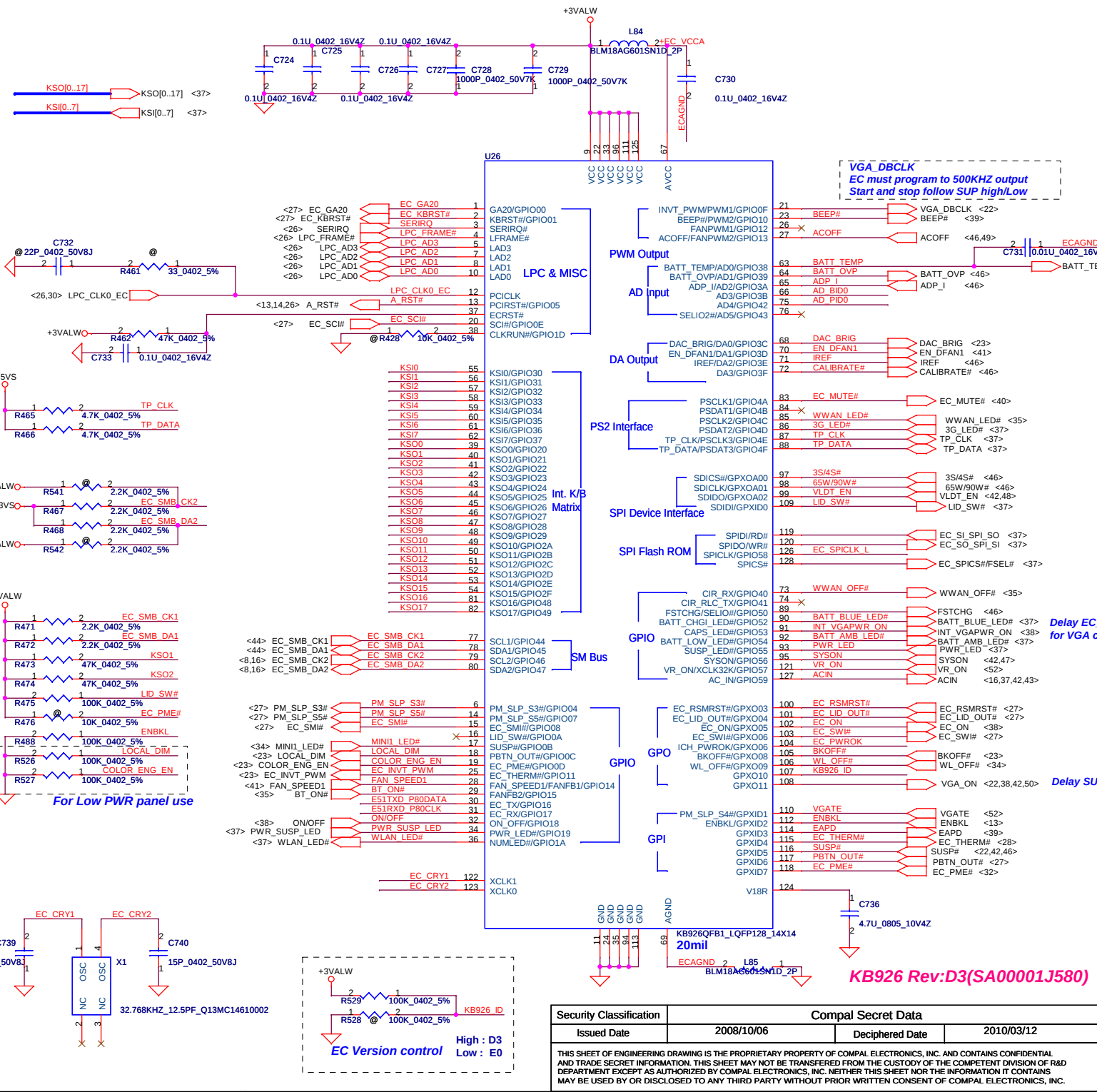
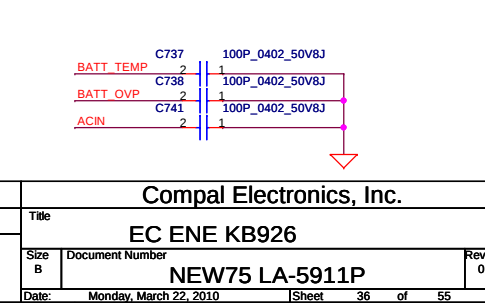
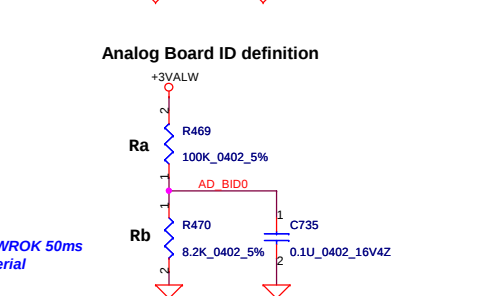
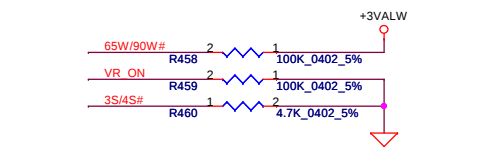
To 3G Module Connect



Bluetooth Conn.

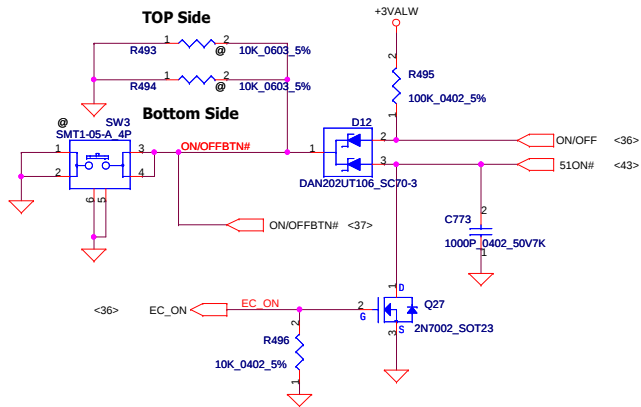


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				0.1	
				Date:	Monday, March 22, 2010
				Sheet	35 of 55

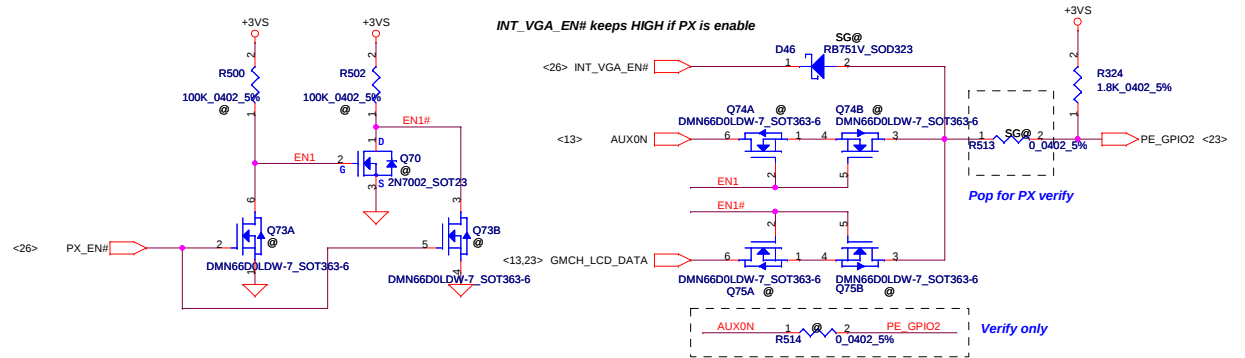


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				Date: Monday, March 22, 2010			Sheet 36 of 55

ON/OFF switch **Power Button**

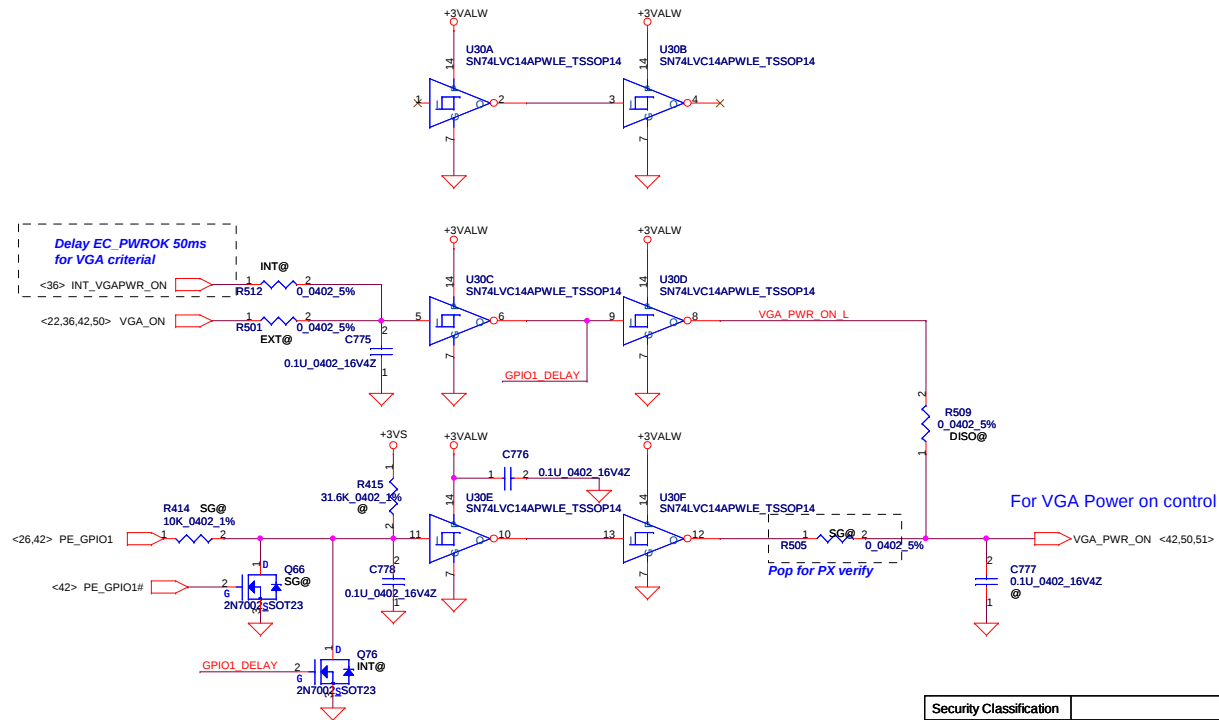


PX MODE SELECT CONTROL <AMD Suggestion>

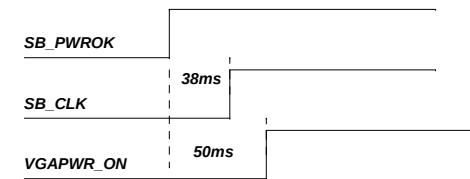


	PX_EN#	AUX0N EDP_DISABLED	I2C_DATA EDP_ENABLED	INT_VGA_EN#	DISPLAY OUTPUT
IGP only mode	1	X	X	0	IGP(LVDS,EDP,VGA,DP)
VGA only mode	1	X	X	1	VGA(LVDS,EDP,CRT,DP)
PX (MUXED)	0	0/1	0/1	1	VGA/IGP(CRT, LVDS, EDP); MXM(DP)
PX (MUXLESS)	0	X	X	0	IGP(LVDS,EDP,CRT,DP)

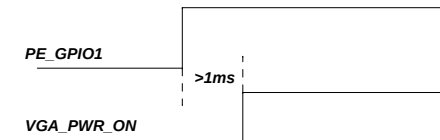
VGA Power ON Circuit



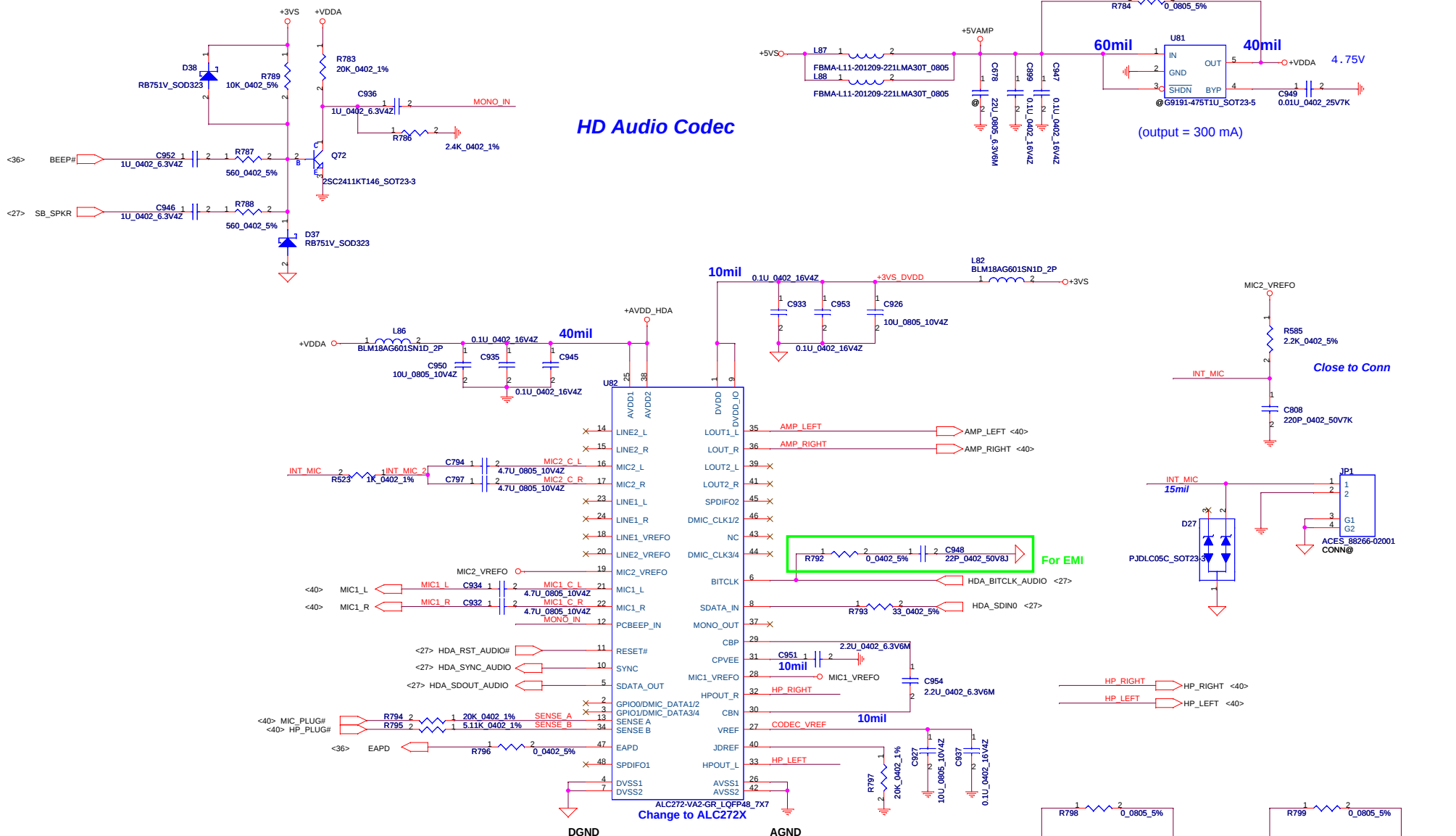
For PX sequence and internal clock mode, VGA PWR need ramp up after SB_CLK oscillate



For PX sequence, >1mS delay is required between
PE_GPIO1 and VGA_PWR_ON



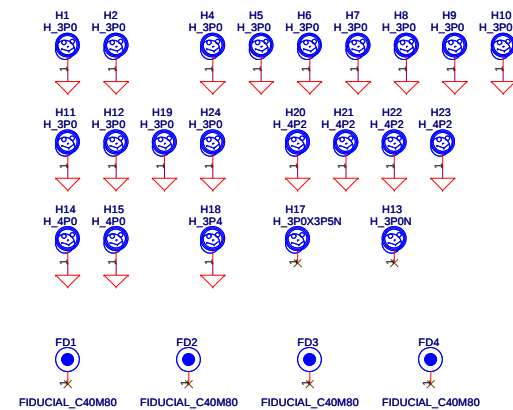
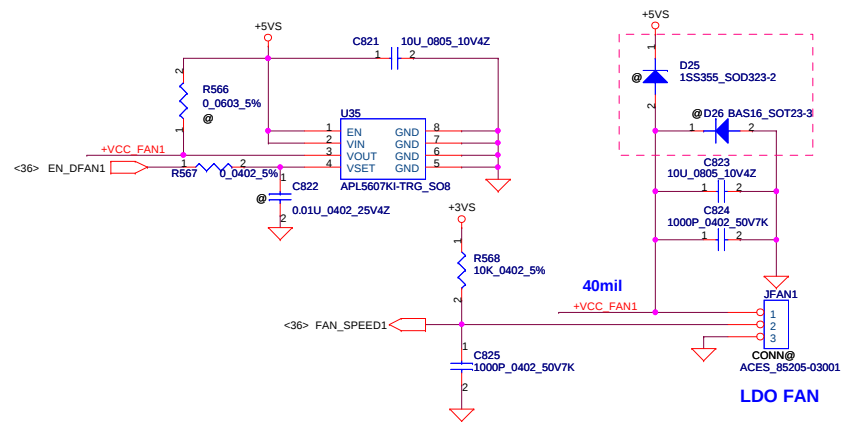
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				Size B	Document Number	Rev 0.1
				NEW75 LA-5911P		
Date: Monday, March 22, 2010				Sheet 38 of 55		



ALC272X			
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	LOUT2
	20K	PORT-B (PIN 21, 22)	MIC1
	10K	PORT-C (PIN 23, 24)	LINE1
	5.1K	PORT-D (PIN 35, 36)	LOUT1
SENSE B	39.2K	PORT-E (PIN 14, 15)	LINE2
	20K	PORT-F (PIN 16, 17)	MIC2
	10K		
	5.1K	PORT-J (PIN 32, 33)	HP

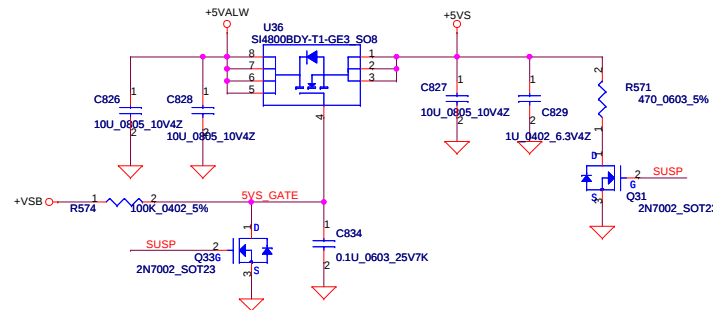
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Size	B	Document Number	NEW75 LA-5911P	Rev	0.1
Date:	Monday, March 22, 2010	Sheet	39	of	55

FAN1 Conn

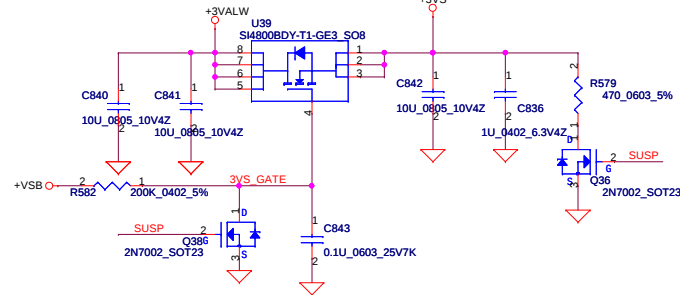


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				Size B	Document Number	Rev
				NEW75 LA-5911P		0.1
Date: Monday, March 22, 2010				Sheet	41	of 55

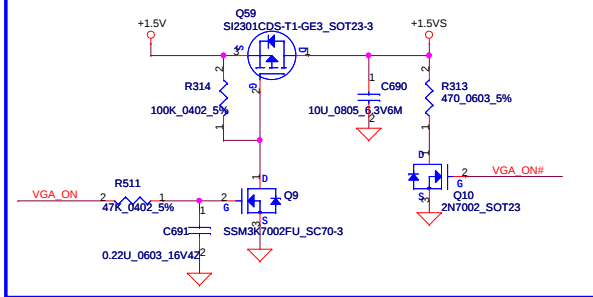
+5VALW TO +5VS



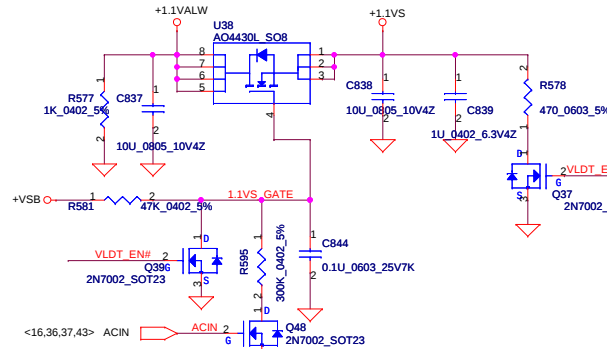
+3VALW TO +3VS



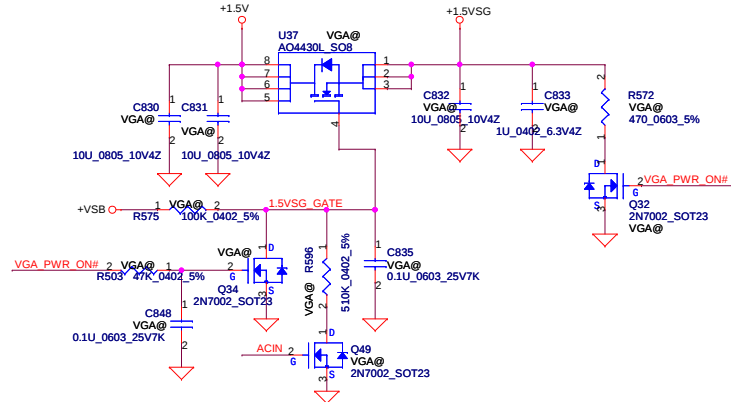
+1.5VS



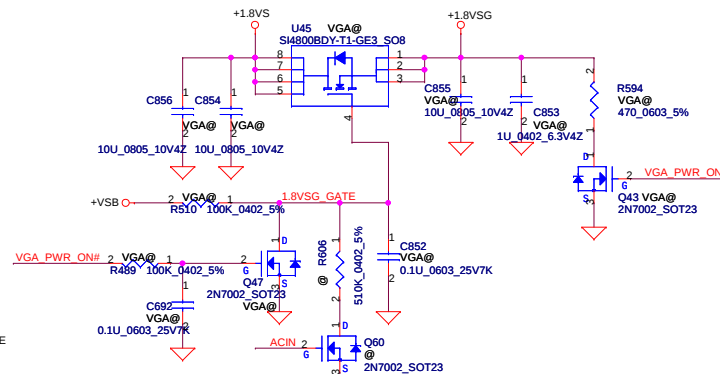
+1.1VALW TO +1.1VS



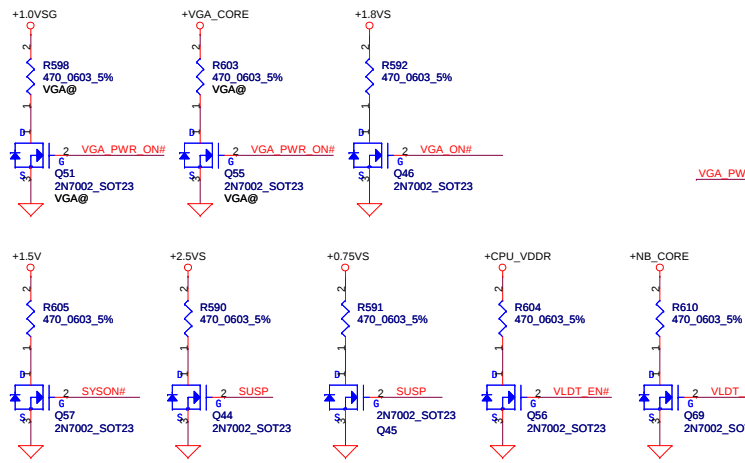
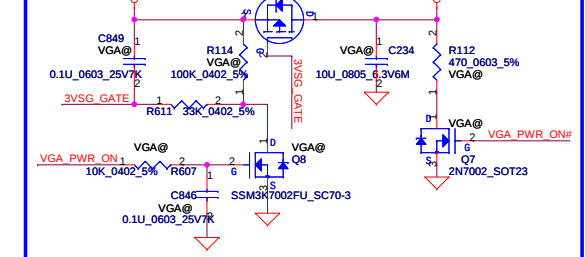
+1.5V to +1.5VSG



+1.8VS to +1.8VSG

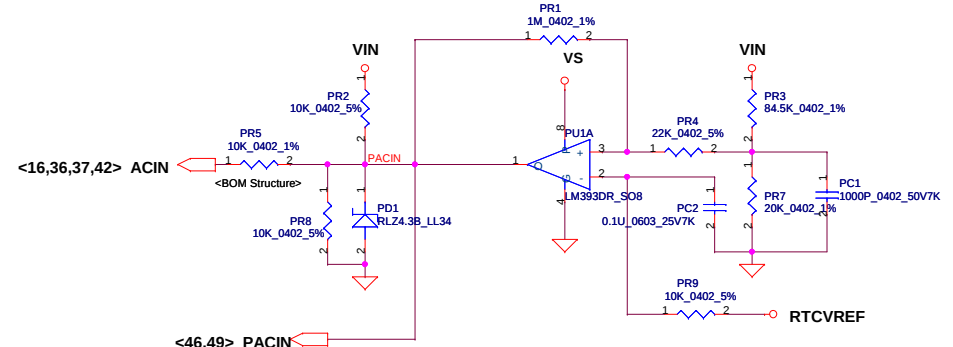
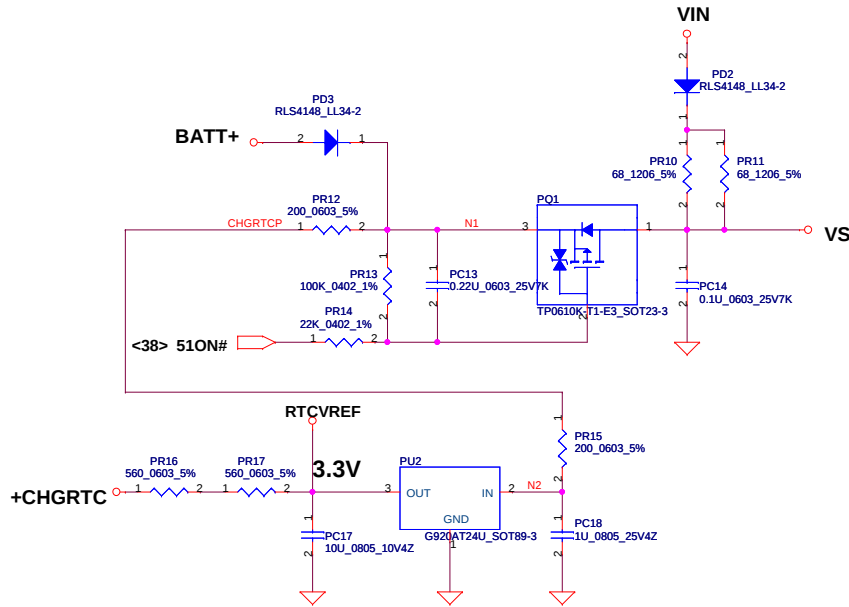
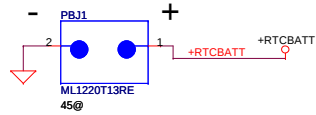
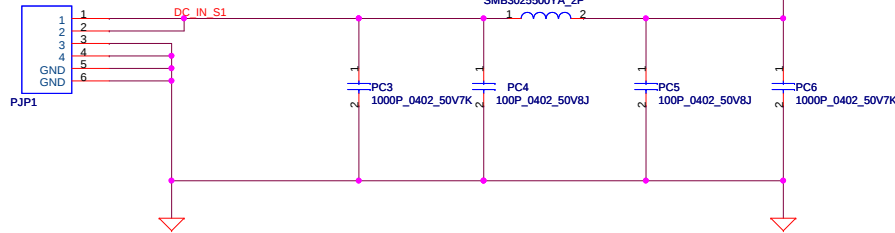


+3VSG

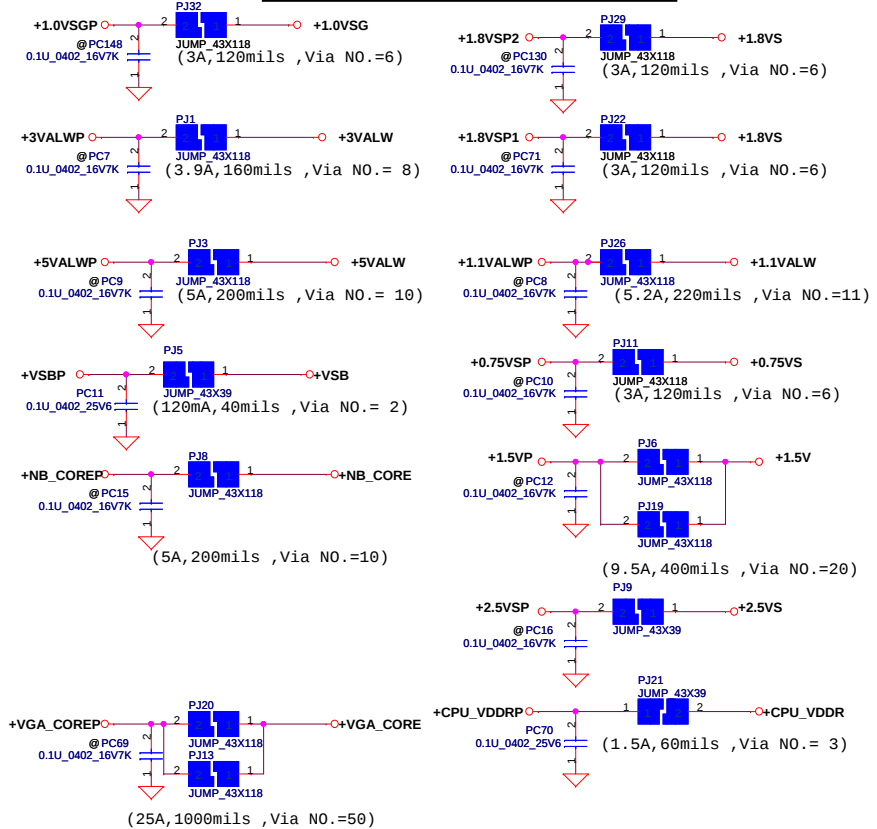


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				NEW75 LA-5911P	
				Date: Monday, March 22, 2010	Rev 0.1
				Sheet 42 of 55	

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ACES_50305-00441-001

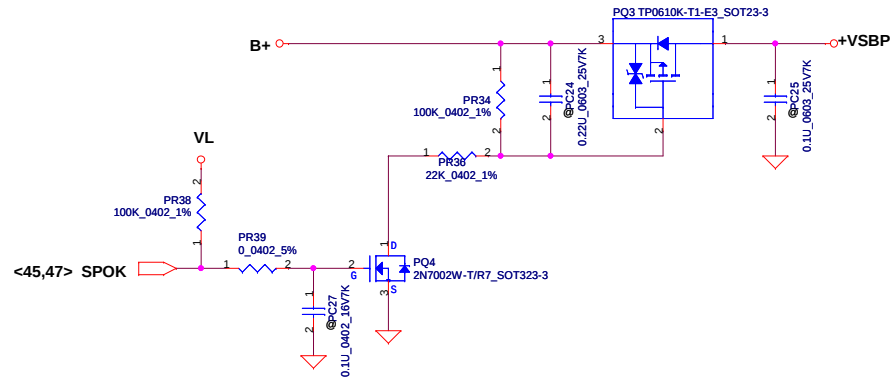
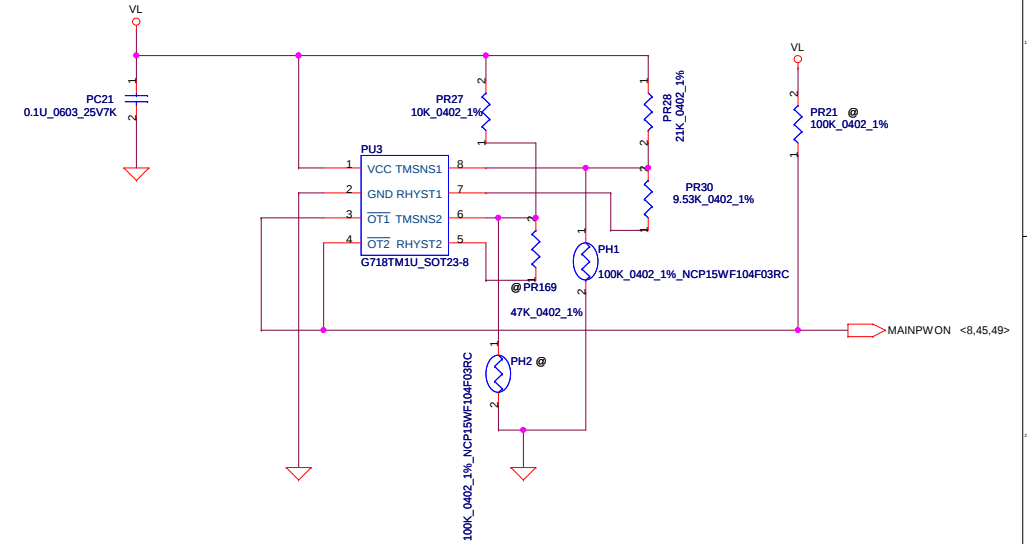
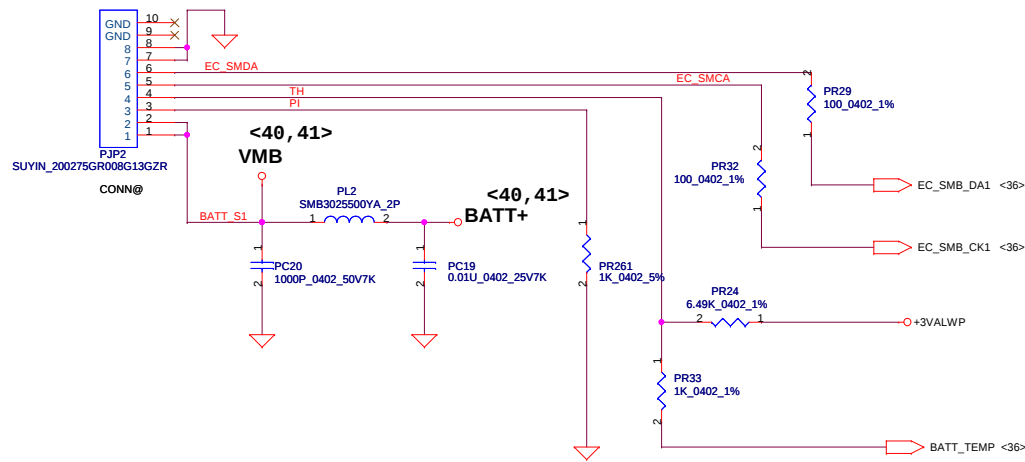


	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

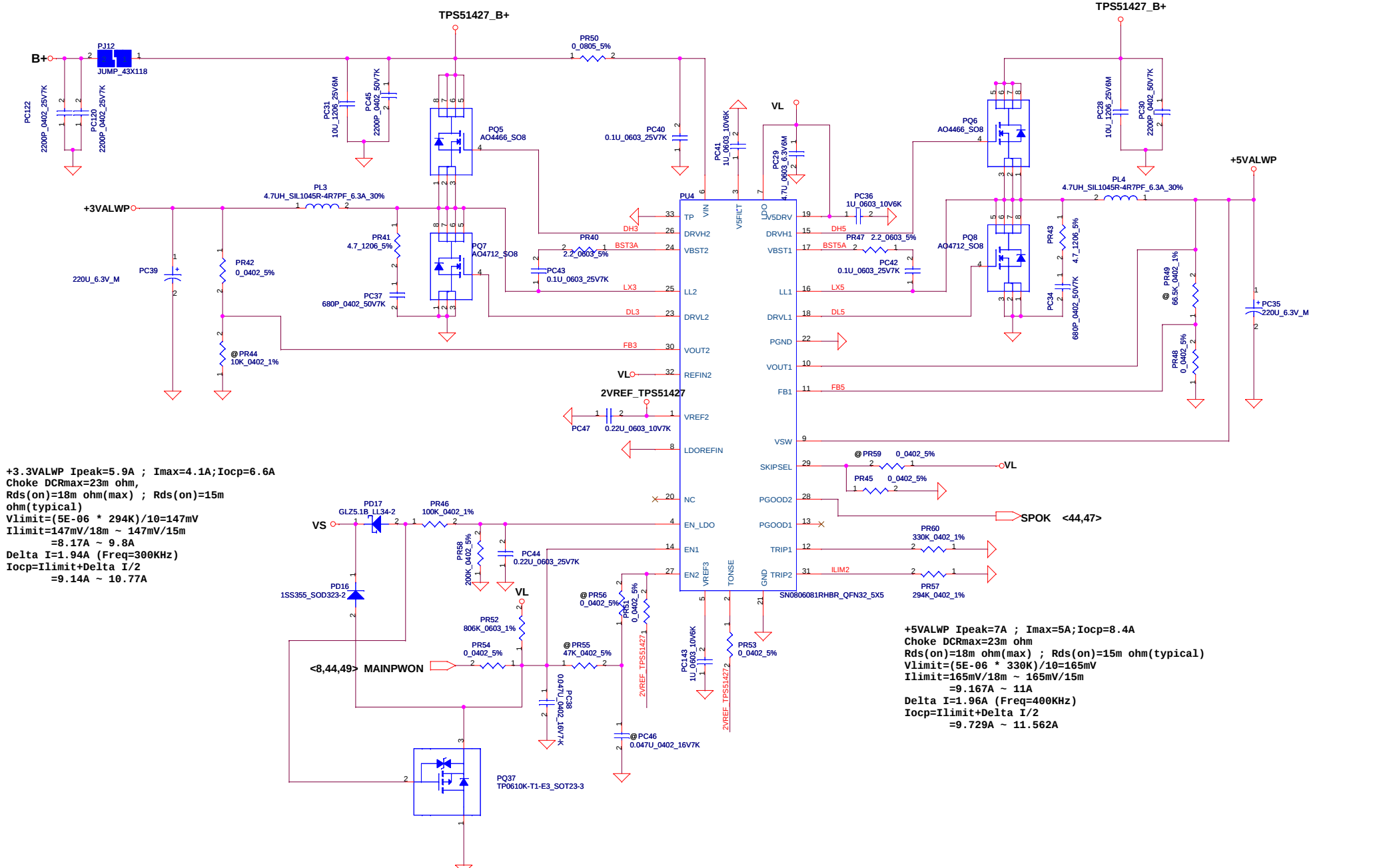


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				Size	Document Number	Rev
				Custom	NAV71 LA-5911P	0.1
				Date:	Monday, March 22, 2010	Sheet 43 of 55

PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



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				Size	Document Number	Rev
				Custom	NAV71 LA-5911P	0.1
				Date:	Monday, March 22, 2010	Sheet 44 of 55



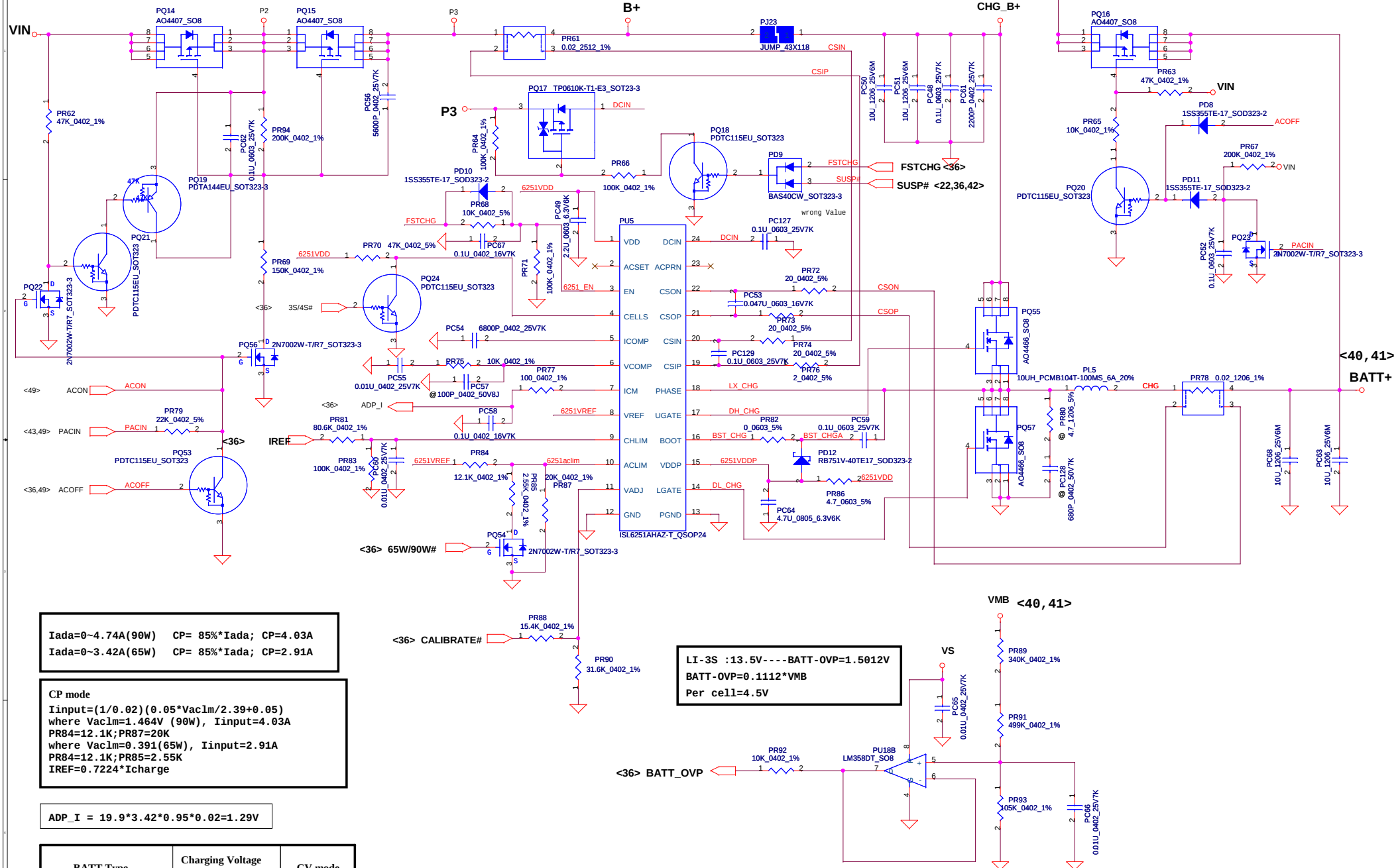
+3.3VALWP Ipeak=5.9A ; Imax=4.1A;Iocp=6.6A
Choke DCRmax=23m ohm,
Rds(on)=18m ohm(max) ; Rds(on)=15m
ohm(typical)
Vlimit=(5E-06 * 294K)/10=147mV
Ilimit=147mV/18m ~ 147mV/15m
=8.17A ~ 9.8A
Delta I=1.94A (Freq=300KHz)
Iocp=Ilimit+Delta I/2
=9.14A ~ 10.77A

+5VALWP Ipeak=7A ; Imax=5A;Iocp=8.4A
Choke DCRmax=23m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Delta I=1.96A (Freq=400KHz)
Iocp=Ilimit+Delta I/2
=9.729A ~ 11.562A

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				Custom	NAV71 LA-5911P
				Date	Monday, March 22, 2010
				Sheet	45 of 55
				Rev	0.1

Iada=0~4.74A(90W/19V=4.736A)

CP = 85%*Iada ; CP = 4.03A



Iada=0~4.74A(90W) CP= 85%*Iada; CP=4.03A
Iada=0~3.42A(65W) CP= 85%*Iada; CP=2.91A

CP mode
Iinput=(1/0.02)(0.05*Vacm/2.39+0.05)
where Vacm=1.464V (90W), Iinput=4.03A
PR84=12.1K; PR87=20K
where Vacm=0.391(65W), Iinput=2.91A
PR84=12.1K; PR85=2.55K
IREF=0.7224*Icharge

ADP_I = 19.9*3.42*0.95*0.02=1.29V

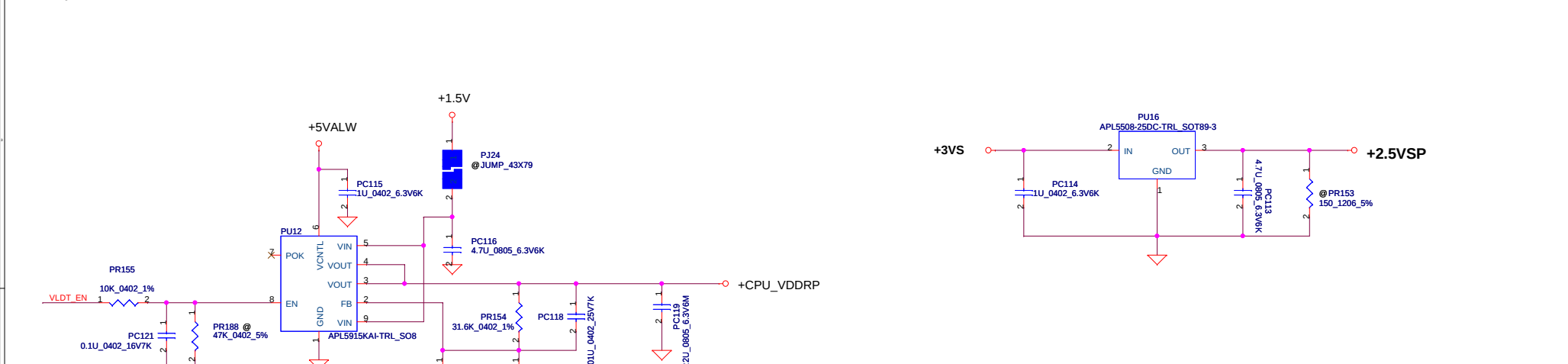
LI-3S :13.5V---BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=4.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

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				Custom		0.1
				Date:	Monday, March 22, 2010	Sheet 46 of 55

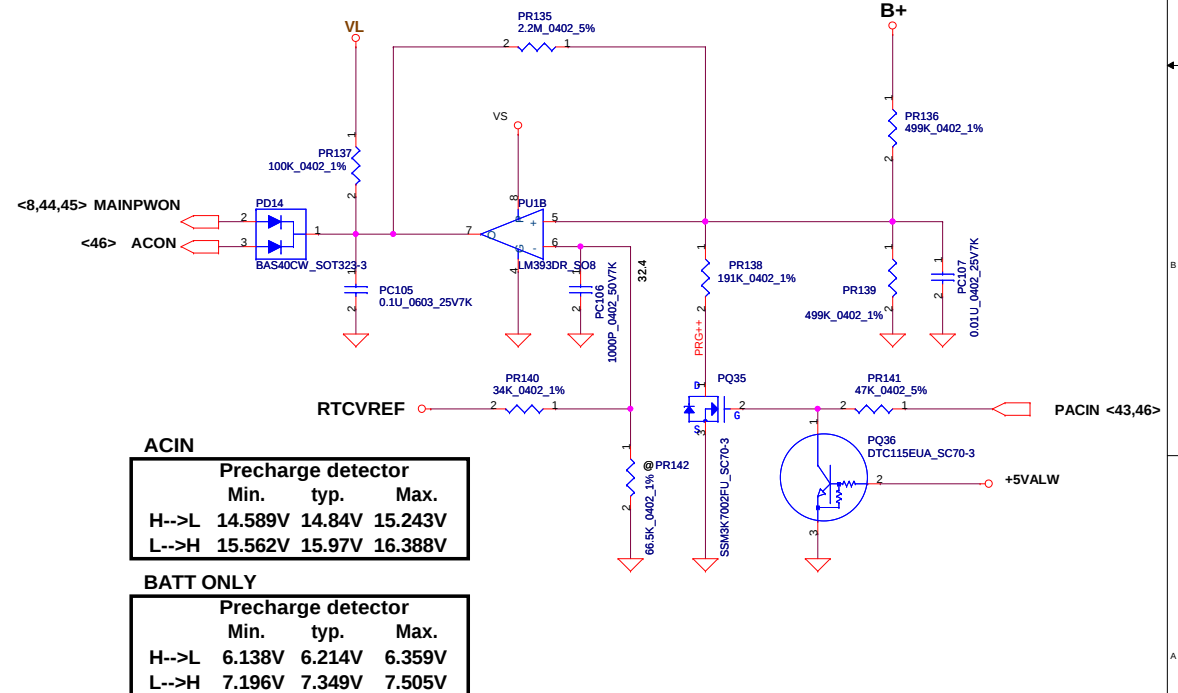
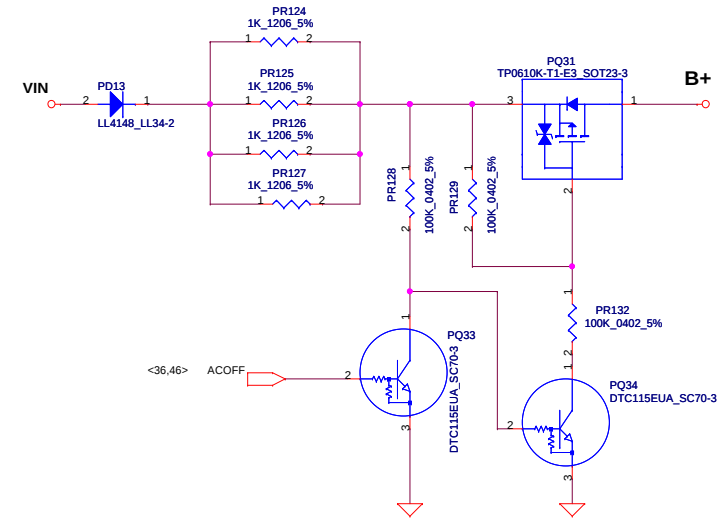
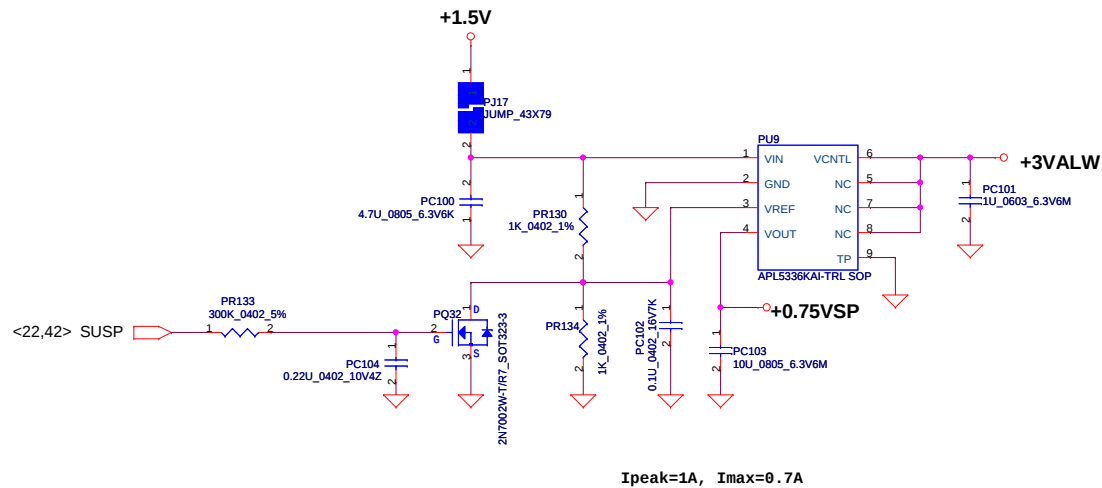
	POWER_SEL
HIGH	0.95V
LOW	1.1V

$V_o = 1.1V$ $V_{FB} = 0.75V$
 $V = 0.75 * (1 + 4.7K/10K) = 1.1V$
 $F_{sw} = 280KHz$
 $C_{out} ESR = 15m\ \Omega$ $R_{dson(max)} = 18m\ \Omega$ $R_{dson(typ)} = 15m\ \Omega$
 $I_{peak} = 7.6A$, $I_{max} = 5.4A$, $I_{ocp} = 9.2A$
 $\Delta I = ((19 - 1.1) * (1.1/19)) / (L * F_{sw}) = 2.06A$
 $\Rightarrow 1/2 \Delta I$ $I = 1.03A$
 $V_{tripmax} = I_{ocp} * R_{dson} = 9.2 * 5.6 * 1.3 = 0.067V$
 $R_{cs} = V_{trip} / 9uA = 0.067V / 9uA = 7.44K$
 choose $R_{cs} = 7.5K$
 $I_{ocpmax} = ((7.5K * 11uA) / (0.0045)) + 1.03A = 19.36A$
 $I_{ocpmin} = ((7.5K * 9uA) / (0.018 * 1.3)) + 1.03A = 10.3A$
 $I_{ocp} = 10.3A - 19.36A$

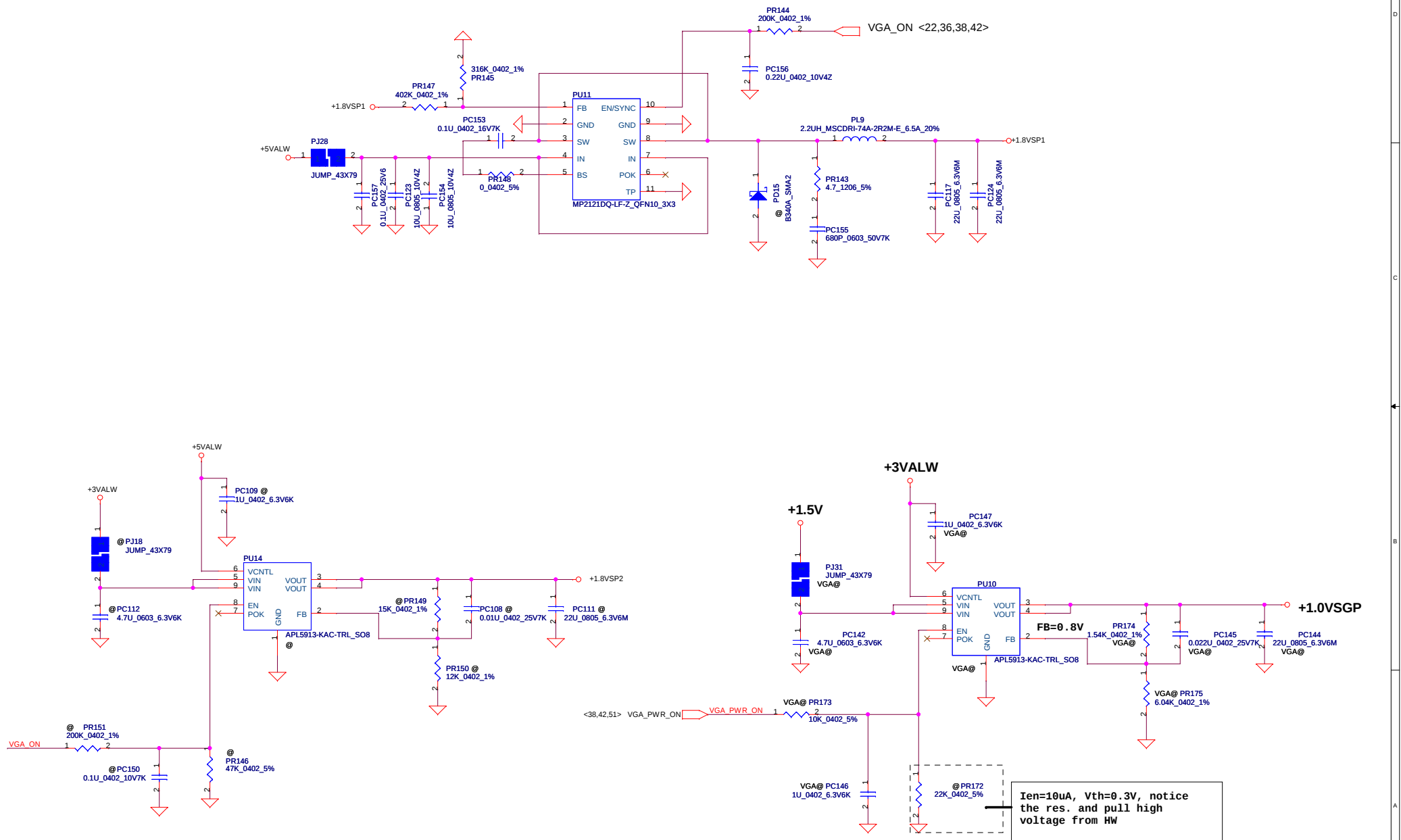


	VDDR_SW
HIGH	1.05V
LOW	0.9V

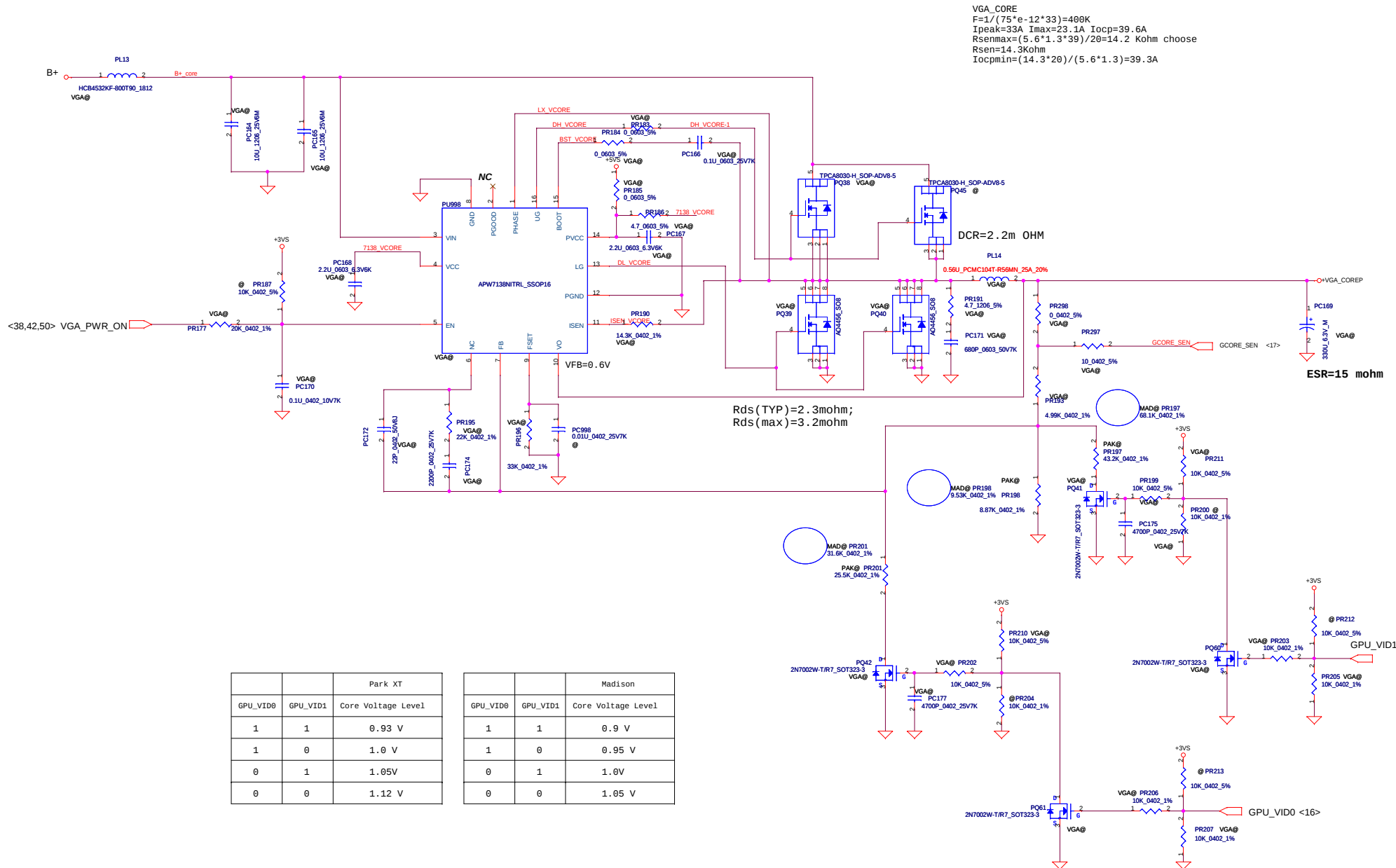
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				Custom	NAV71 LA-5911P	
				Date:		Monday, March 22, 2010



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Issued Date		2007/09/20		Deciphered Date		2010/03/12		Title	
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		Size Custom	Document Number						Rev
		NAV71 LA-5911P						0.1	
		Date:	Monday, March 22, 2010			Sheet	49	of	55



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Size	Custom	Document Number	NAV71 LA-5911P		Rev B
Date:	Monday, March 22, 2010	Sheet	50	of	55



Park XT		
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.93 V
1	0	1.0 V
0	1	1.05V
0	0	1.12 V

Madison		
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.9 V
1	0	0.95 V
0	1	1.0V
0	0	1.05 V

Version change list (P.I.R. List)

Page 1 of 2
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ADD 2 switch mos and remove 2 pull high resistance to modify VGA_CORE switch level	Before modify to fault, we recognize that VGAPWRSEL pin is open drain state. But after check with AMD AE regoer to clear the foul that VGAPWRSEL pin has driving ability.so i take away 2 pull high resistance and add 2 switch mos to modify the switch level.	0.1	52	ADD PQ60 and PQ61 remove PR212(10K,0402) and PR213(10K.0402)	2009/08/21	EVT_NEW75
2	change thermister , tune PH1 protection and recovery set point	change thermister from 150K to 100K	0.1	44	thermister part number SL200000V00 and PR28 change to 21K, PR30 change to 9.53K	2009/08/27	EVT_NEW75
3	Add GPU voltagr sence net	Cause GPU have GCORE_SEN and FB_GND pin so power add receive net.	0.1	51	ADD GCORE_SEN and FB_GND net, also add PR296(0_0402_1%), PR297(10_0402_5%) and PR298(0_0402_5%)	2009/09/04	EVT_NEW75
4	change DC-IN connector part number	to meet pin definition	0.1	43	change part number is SP020908120	2009/09/10	EVT_NEW75
5	change reistance PR81 value	Cause meet battery Ki value setting from 1.106 to 0.7224. change PR81 from 154K(0402_1%) to 80.6K(0402_1%)	0.1	46	change resistance PR81 value from 154K to 80.6K	2009/09/22	EVT_NEW75
6	ADD switch circuit for 1.05V	Cause follow AMD electrcial sheet, VDDIO/ VDDR voltage setting procedure. AMD processor will switch between 1.05V and 0.9V by VDDIO and VDDR	0.1	48	ADD PR161 (165K_0402_1%), PQ58, PR152(10K_0402_5%), PR160(10K_0402_5%), PC131(0.1U_25V6) , change PR161 value from 100K to 249K, and ADD enable net name -VDDR_SW	2009/09/22	EVT_NEW75
7	change resistance size	cause for component de-rating . Prevent the component break down when inrush current happen.	0.1	46	change PR61 from (0.02_1206_1%) to (0.02_2512_1%)	2009/10/06	EVT_NEW75
8	Modify VGA_CORE mapping table.	cause ATI change power play voltage, so change the table value.	0.1	51	change PR198 from 9.76_0402_1% to 9.53_0402_1%, PR197 from 37.4_0402_1% to 64.9_0402_1% and PR201 from 17.8_0402_1% to 31.6_0402_1%	2009/10/06	EVT_NEW75
9	Change 1.0VSGP enable RC value	Prevent LDO can't turn off when it should turn off	0.1	50	Change PR173 from 100K_0402_5% to 10K_0402_5%, PC146 from 0.1u_0402 to 1u_0402	2009/10/15	EVT_NEW75
10	Change lowside MOS of VGA_CORE	Cause light load efficiency result is fail, and we get result after discuss FAE. The reason is lowside mos Rdson too less and IC will detect not very sensitive	0.1	51	Change PQ39 and PQ40 from TPCA8028(SB00000GL00) to A04456(SB000009F80)	2009/11/19	EVT_NEW75
11	Change 3/5Valw boost resistance value	For EMI request	0.1	45	Change PR40 and PR47 from 0_0603_5% to 2.2_0603_5%(SD013220B80)	2009/11/19	EVT_NEW75
12	ADD two capacity	For EMI request	0.1	52	Add pc219 and pc220 are both S CER CAP 1000P 50V K X7R 0402	2009/11/23	EVT_NEW75
13	ADD three resistance	Cause madison and park need different voltage switch level so add different resistance value for the problem.	0.1	51	Add PR197(68.1K_0402_1%) , PR198 (9.53K_0402_1%) and PR201 (31.6K_0402_1%)	2009/11/23	EVT_NEW75
14	Change chock	Cause A phase put wrong chock	0.2	37,39,40	Change PL9 from SH00000FK00 to SH000009Q00	2009/11/23	EVT_NEW75

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Size				Document Number	Rev
Custom				NAV71	0.1
Date:				Monday, March 22, 2010	Sheet 53 of 55

Version change list (P.I.R. List)

DVT Stage

- 1. remove Y4 related
- 2. add a bead on +VDDA11PCIE ---ok (add L28)
- 3. use 6mohm MOS on +1.1VS ---ok (U38,U37)
- 4. +1.1VALW vlotage level --check PW rail
- 5. check EC sequence (syson/vga_on) --ok
- 6. VRAM ID --ok
- 7. VRAM_RST circuit -- check slew rate
- 8. 3G module circuit update --ok
- 9. EC 500K circuit --ok
- 10. MEMZN circuit (0ohm/10uF) --ok
- 11. check GBE PU/PPD --ok
- 12. check capacitor size
- 13. TXC crystal value --ok (change X1,Y2), Y5
- 14. internal clock circuit --ok
- 15. ADD VGAPWR_ON --ok, INT_VGAPWR_ON
- 16. define PX_FN/CLK_MODE strap pin --ok
- 17. define CLK_REQ for internal CLKREQ --ok
- 18. change 4.7u_0805 type --ok
- 19. BOM change for SG --ok
- 20. add VGAPWR_ON for SG&int clock use --ok
- 21. add PJ25 --ok
- 22. LED1/3 680ohm, LED2/4 3.9Kohm --ok
- 23. add MUXLESS strap --ok (R521,R612)
- 24. add LPW planel feature --ok (LOCAL_DIM / COLOY_ENG_EN)
- 25. EC version control--ok (R529,R528)
- 26. WiMAX LED combine circuit --ok (R530,R531,D47)
- 27. change INT_VGAPWR_ON to EC_pin91 --ok
- 28. add VB function --ok (R533,R532)
- 29. Add R534,R535,R536 for layout --ok
- 30. change Y5 to 33p cap
- 31. pop ESD diode --ok
- 32. set T25 to BH for main --ok
- 33. Define Board file ID for SW req. --ok

PVT Stage

- 1. un-pop D39,D41 p.40
- 2. pop D27 p.39
- 3. un-pop Q73,Q74,Q75,Q70,R500,R502 p.38
- 4. Change R470 to 8.2K p.36
- 5. Change R600,R510,R489 to 100K p.22/p.42
- 6. Change C847 to 0.1u p.22
- 7. Change C739,C740 to 15p p.36
- 8. Change LED resistance R477,R499 change to 2.2K p.37
- 9. Change R611 to 33K p.42
- 10. Change HDMI_HPDP PU from +3VSG to +3VS p.24
- 11. Change C957,C971 to 0.47u_0603 p.40
- 12. Remove VGA option solution
unpop R147,R420,R421,R248 pop R161 p.16/p.22/p.17
- 13. Pop R595,R596,Q49,Q48 change R595 to 300k p.42
- 14. Change LED1,LED3 to SC591NB5A30 p.37
- 15. Change Q5,Q26 to SB00000DH00 p.16/p.37
- 16. Change C468~C475 to MAD@ p.20
- 17. Change C305,C306 to 0603 size p.18
- 18. Change LED control circuit, Pop R537,R457 p.34/p.35
- 19. Update AMP GAIN to 10dB p.40
- 20. Change C11,C56,C723 to SGA00002N80 p.8/p.9/p.35
- 21. Change TPC24 to TPC12 for layout

MP Stage

- 1. Add R541, R542 for TSI leakage current issue. (option) p.36
- 2. Change C21 from 3300pF to 100pF
- 3. Unpop C21
- 4. Unpop SW3
- 5. Change C305 to MAD@

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				Size B	Document Number
				NEW75 LA-5911P	
Date: Monday, March 22, 2010		Sheet 54 of 55		Rev 0.1	

Version change list (P.I.R. List)

Page 1 of 2
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
15	Change chock	Cause NB_CORE and 1.1VALW efficiency measurement result fail. so change inductor from 1.8uH to 1.0 uH, and change the tye from ferrite to moding	0.2	47,48	Change PL6 and PL8 from SH000009680 to SH000009U00	2009/12/01	EVT_NEW75
16	Change resistance value	Cause change low side MOS from TPCA8028 to A04456. And there have different Rds(on). then OCP will different, so i need to change ocp setting resistance.	0.2	51	Change PR190 from SD000004100 (S RES 1/16W 8.2K +-1% 0402) to SD00000QM80 (S RES 1/16W 14.3K +-1% 0402)	2009/12/01	EVT_NEW75
17	ADD sunbber	Cause VGA_CORE phase ringing too strong, so add sunbber to reduce the ringing	0.2	51	ADD PR191(SD001470B80 ,S RES 1/4W 4.7 +-5% 1206) and PC171(SE025681K80 S CER CAP 6,80P 50V K X7R 0603)	2009/12/01	EVT_NEW75
18	Change resistance value	change VGA_CORE switch frequency fromm 300K to 400K, for solve efficiency fail issue	0.2	51	Change PR196 from 44.2K to 33K	2009/12/01	EVT_NEW75
19	Delete component PC73, PC83 and PC92	Cause for design resinable	0.2	47,48	Delete PC73,PC83 and PC92	2009/12/01	EVT_NEW75

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				Sheet 55 of 55	